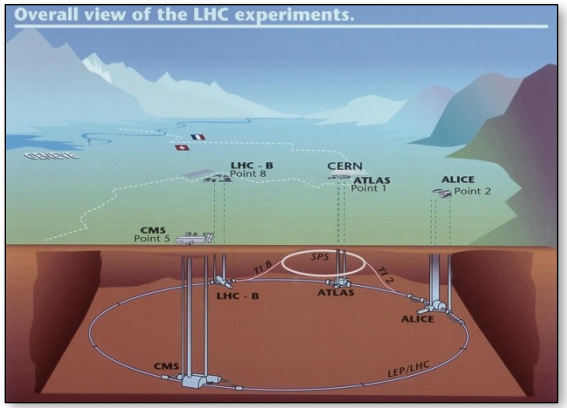
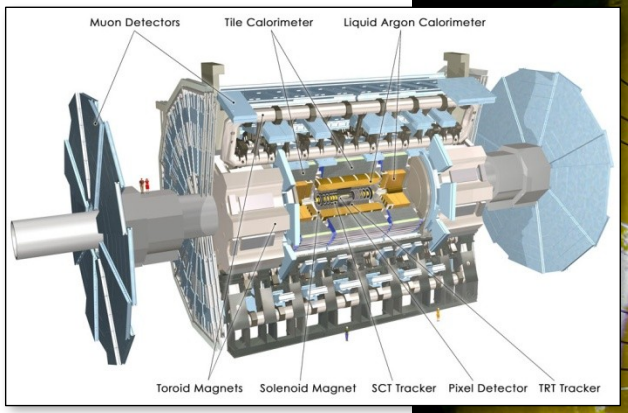
Design analoger Schaltkreise
Vorlesung 1

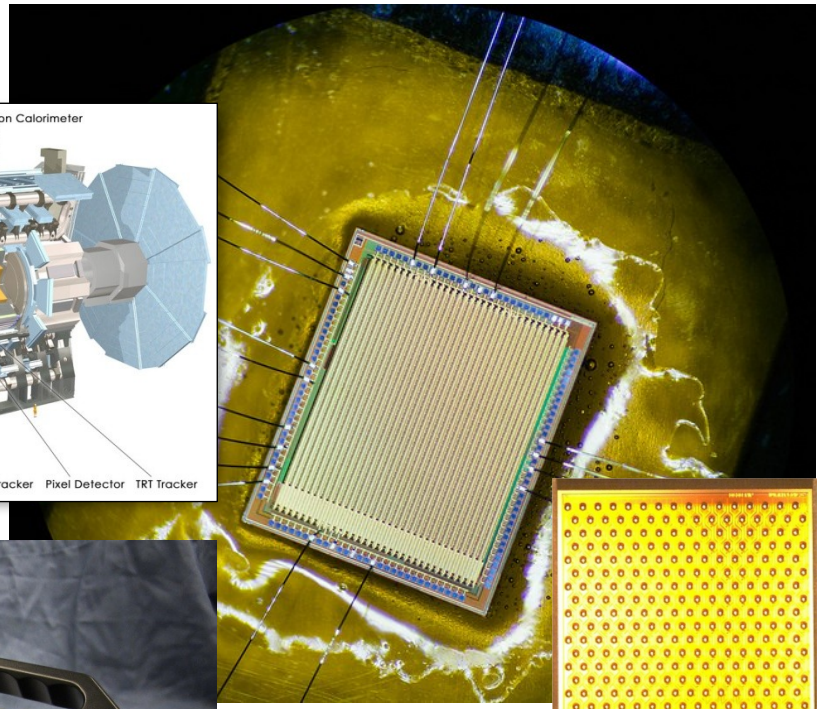
- Institut für Prozessdatenverarbeitung (IPE) am KIT Campus Nord
- ASIC und Detektor Labor
- Detektoren an Teilchenbeschleuniger

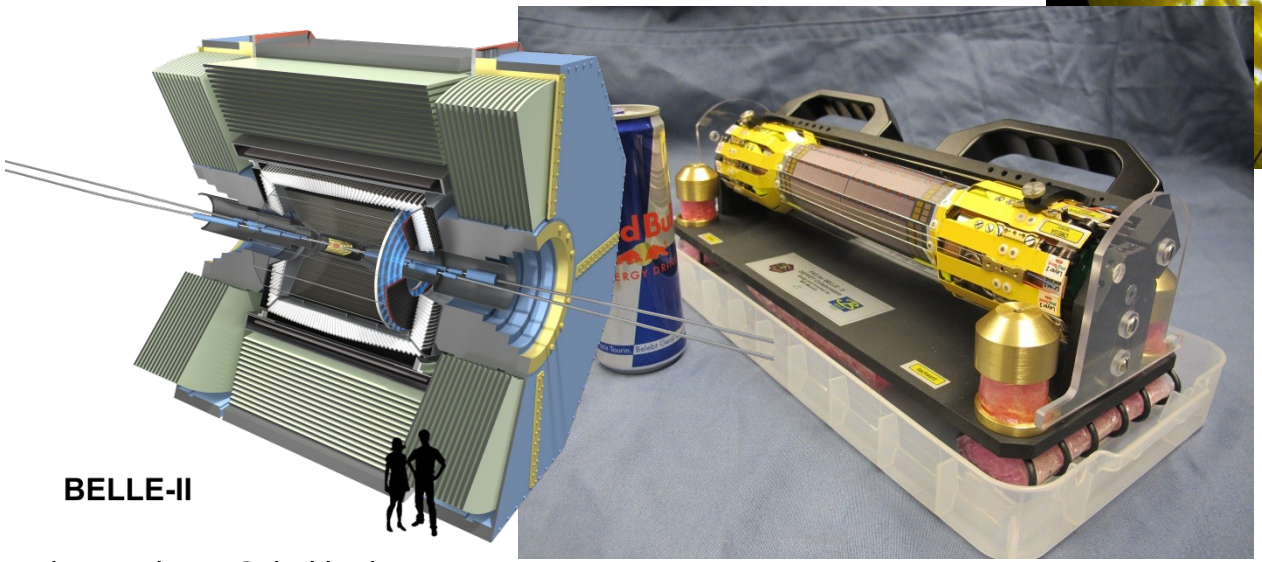
Large Hadron Collider



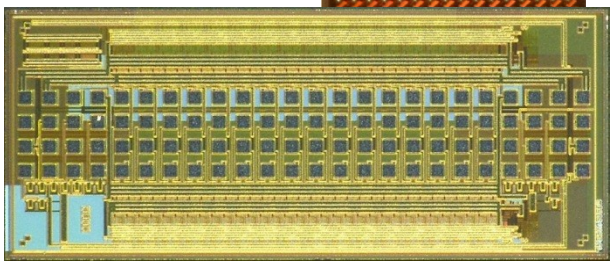
Experiment ATLAS







BELLE-II



Design analoger Schaltkreise

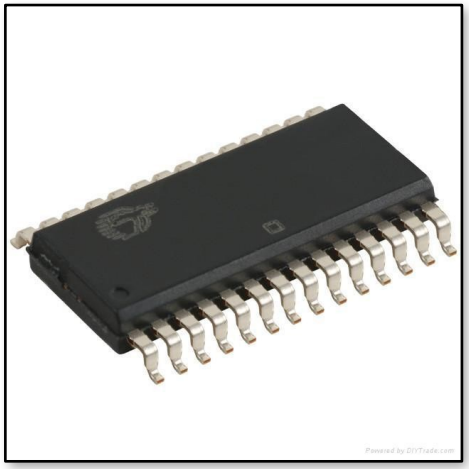
- Vorlesungen und praktische Übungen mit Chipdesign-Software (CIP-Pool am IMS)
- Übungen ab November
- Kontakt: ivan.peric@kit.edu
- Kontakt: richard.leys@kit.edu
- Inhalt ist neu – neue Skripten bald
- https://www.ims.kit.edu/324_201.php

Design analoger Schaltkreise

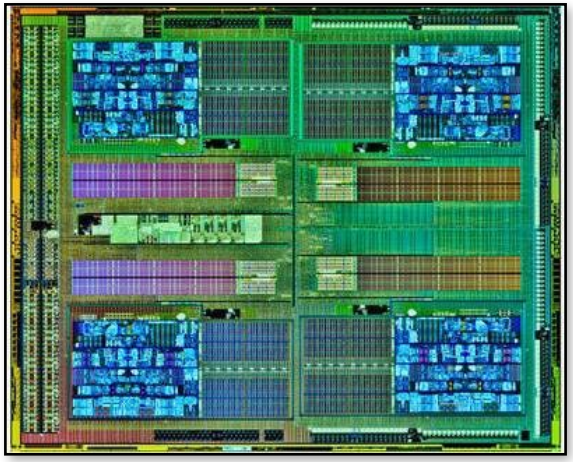
Electronic device

PCB

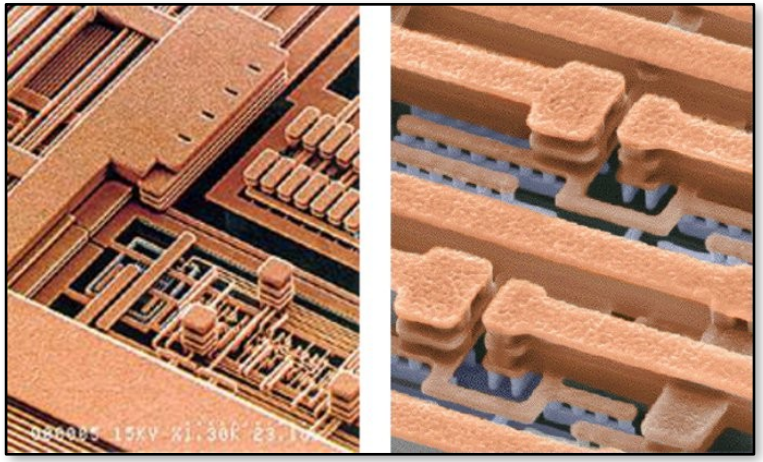
Integrated circuit



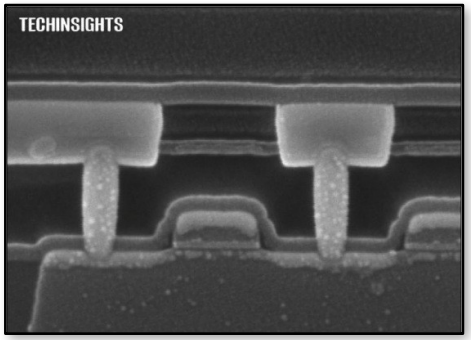
Integrated circuit - core



Interconnection



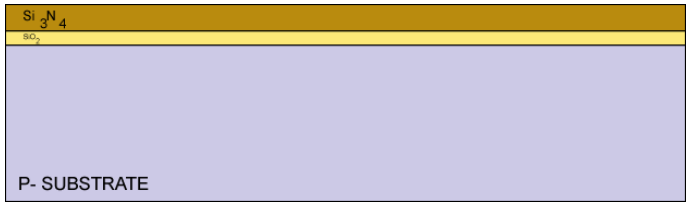
Transistor



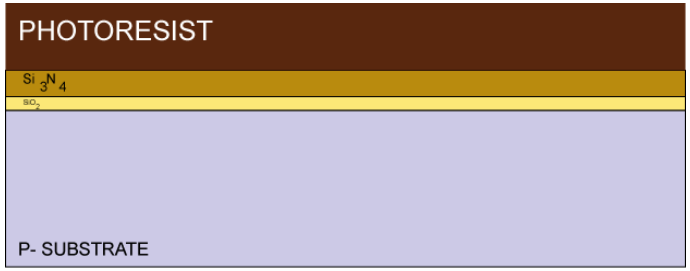
- Vorkenntnisse: Vorlesungen Elektronische Schaltungen und VLSI-Technologie
- MOSFET, JFET, Bipolar-Transistor (BJT)
- Einfache elektronische Schaltungen
- Kleinsignalmodelle, Arbeitspunkt
- Prinzipen der IC Herstellung

- Prinzipen der IC Herstellung
- Wiederholung von Schritten
- Oxid-, Silizium- oder Metalllagen werden auf einem Si-Substrat erzeugt
- Photolithographie (Photolack, UV Licht, trocken- und nassätzen)
- Lagen werden strukturiert
- Silizium wird dotiert
- Link: http://www.halbleiter.org/wie-wird-ein-mikrochip-hergestellt/

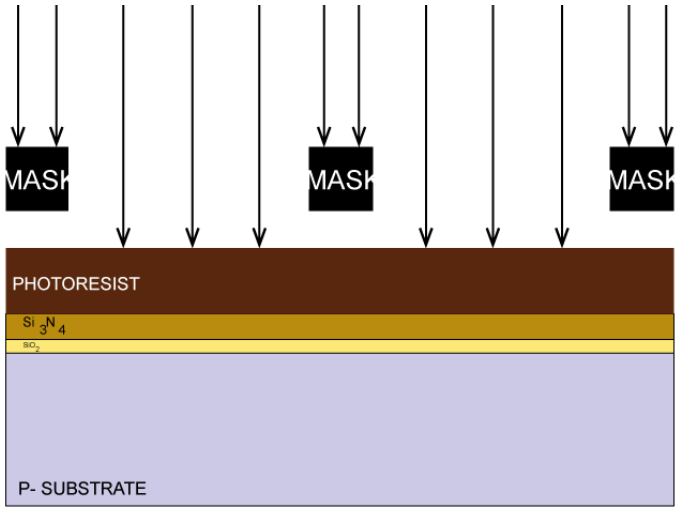
1. Deposition of silicon oxide and nitride



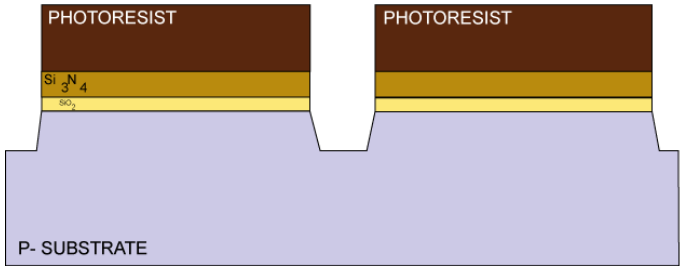
2. Photoresist deposition



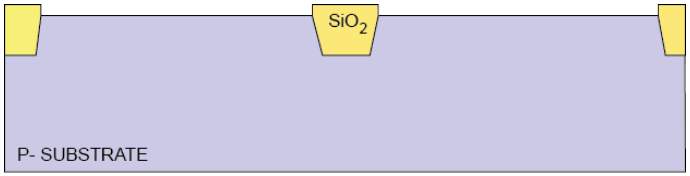
3. Illumination of the photoresist through the mask



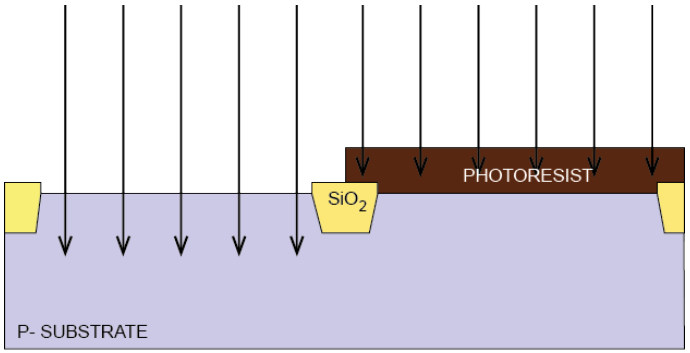
4. Removing illuminated photoresist, etching silicon nitride, etching isolation tranches in silicon



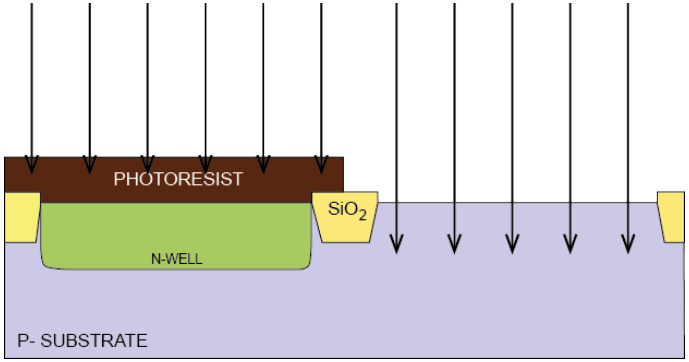
5. Filling isolation trenches with SiO2



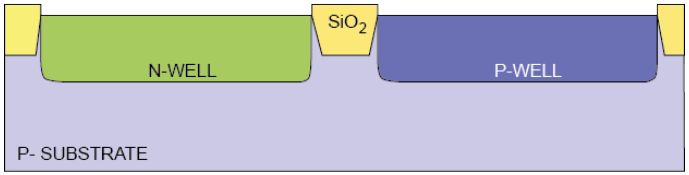
6. Ion implantation (Phosphor ~100 keV) -> N-well formation



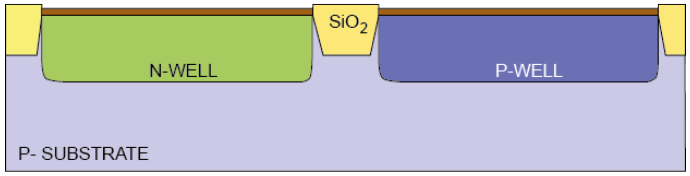
7. Ion implantation (Boron ~100 keV) -> P-well formation



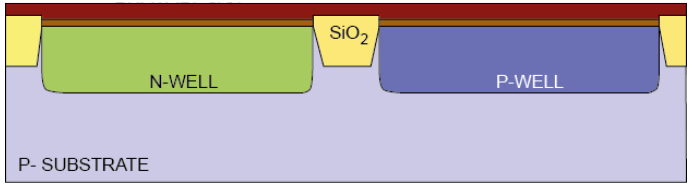
8. N-well and P-well are ready for implementing NMOS and PMOS transistors



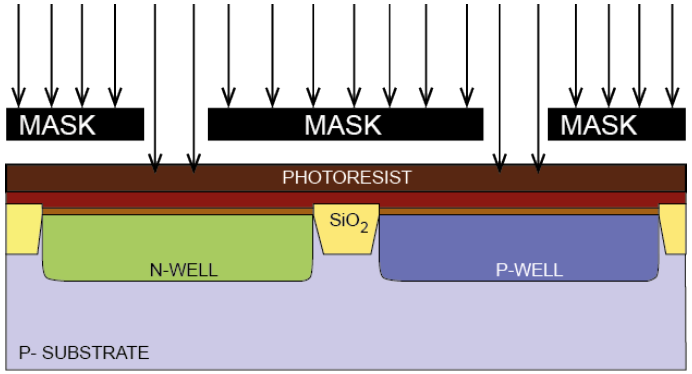
9. Gate oxide deposition



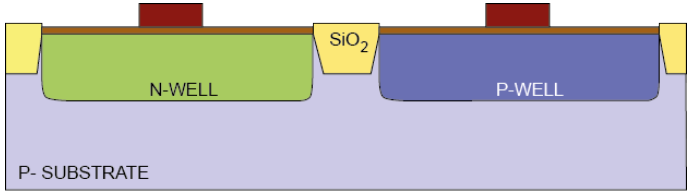
10. Deposition of polysilicon



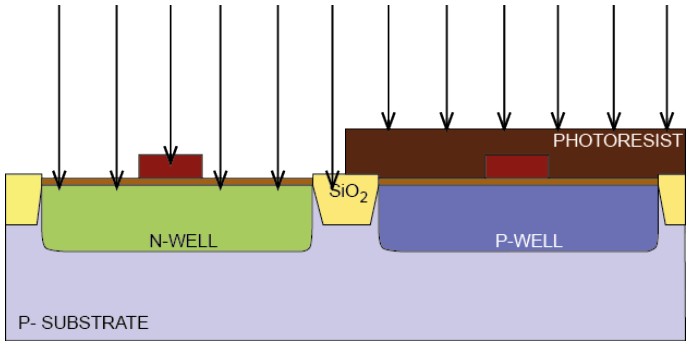
11. Photoresist deposition, illumination through mask



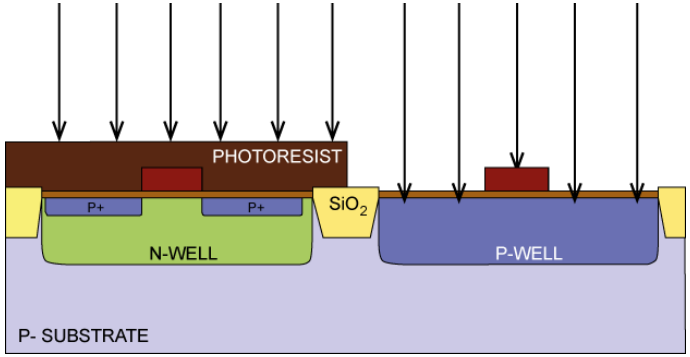
12. Gates are formed



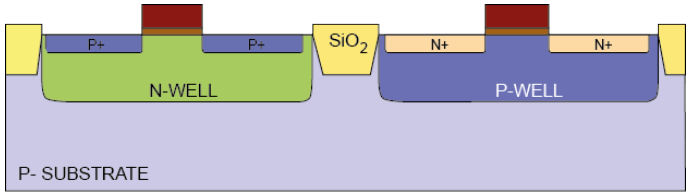
13. Low energy implantation of Boron dopants -> forming P+ regions of drain and source



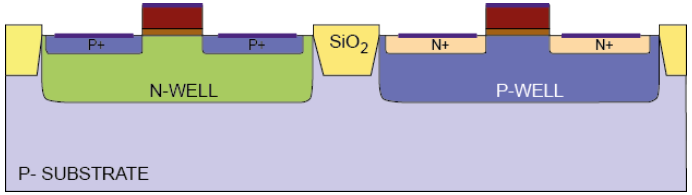
14. Low energy implantation of Phosphor dopants -> forming N+ regions of drain and source



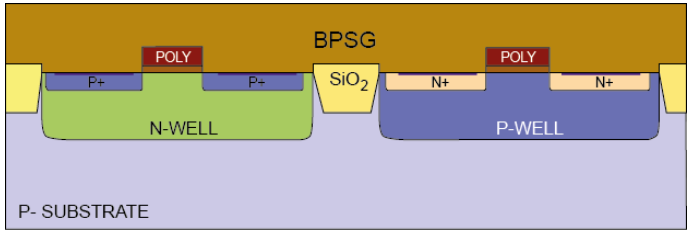
15. Removing photoresist and oxide from source and drain



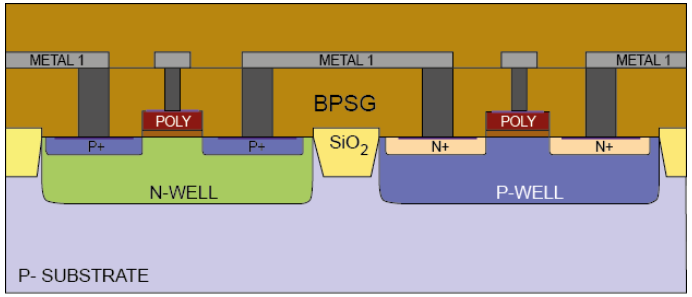
16. Silicidation



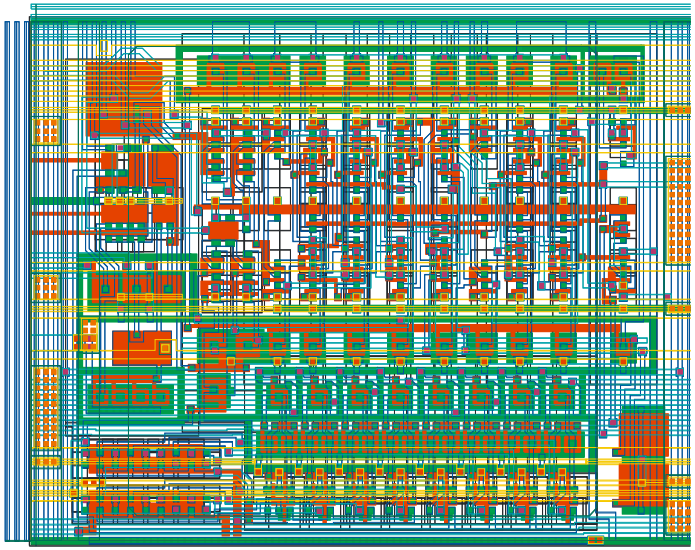
16. BPSG deposition



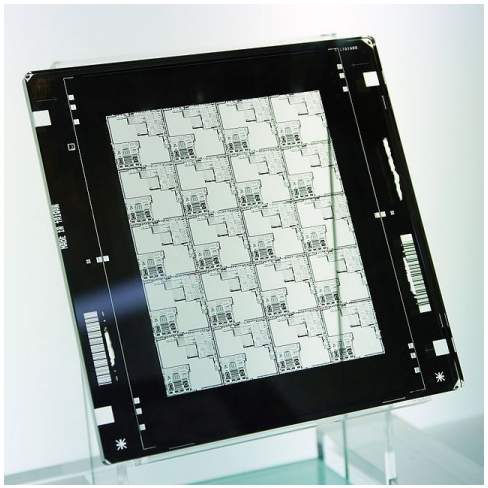
17. Etching, vias, deposition of METAL1, BPSG isolation



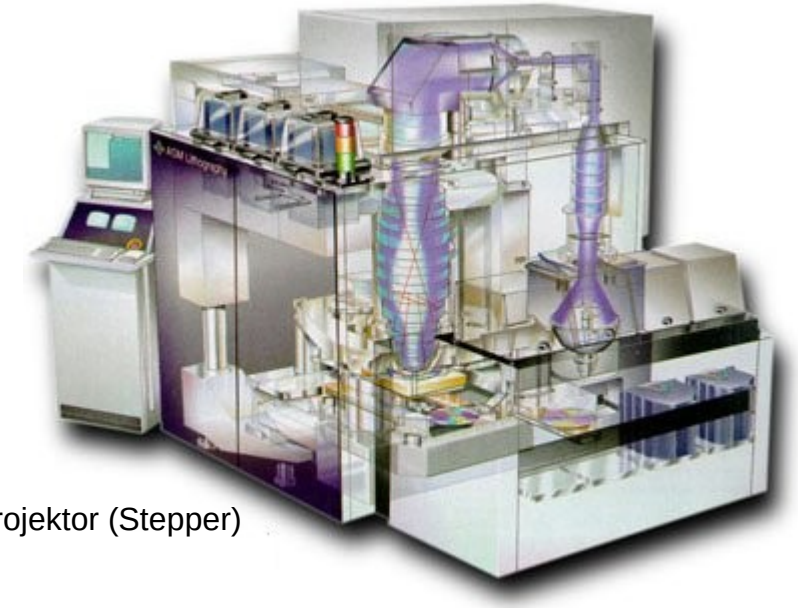
- Layout -> Fotomaske -> IC



Layout

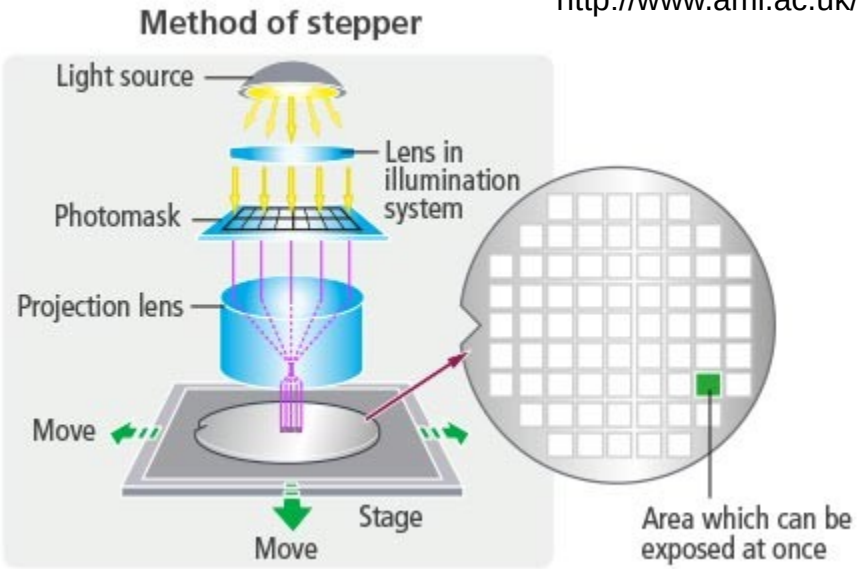


Maske

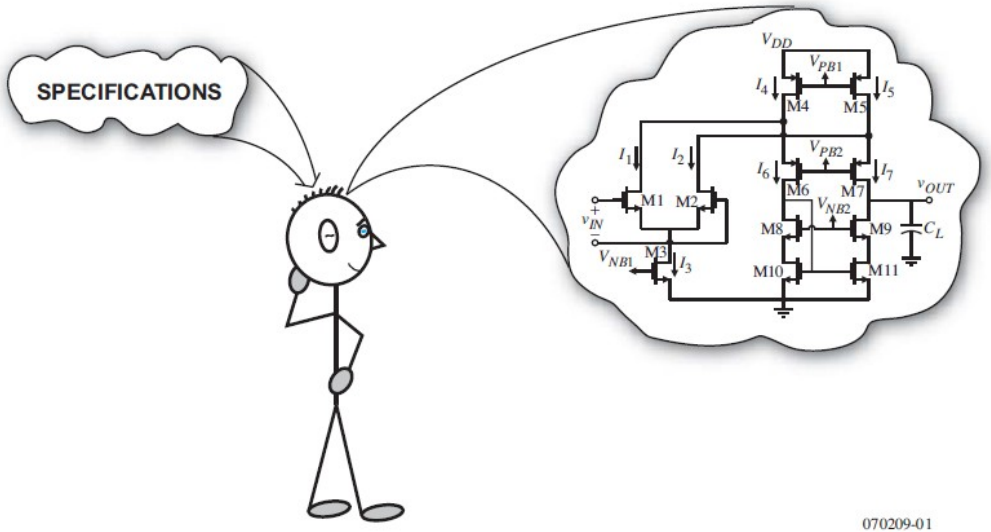


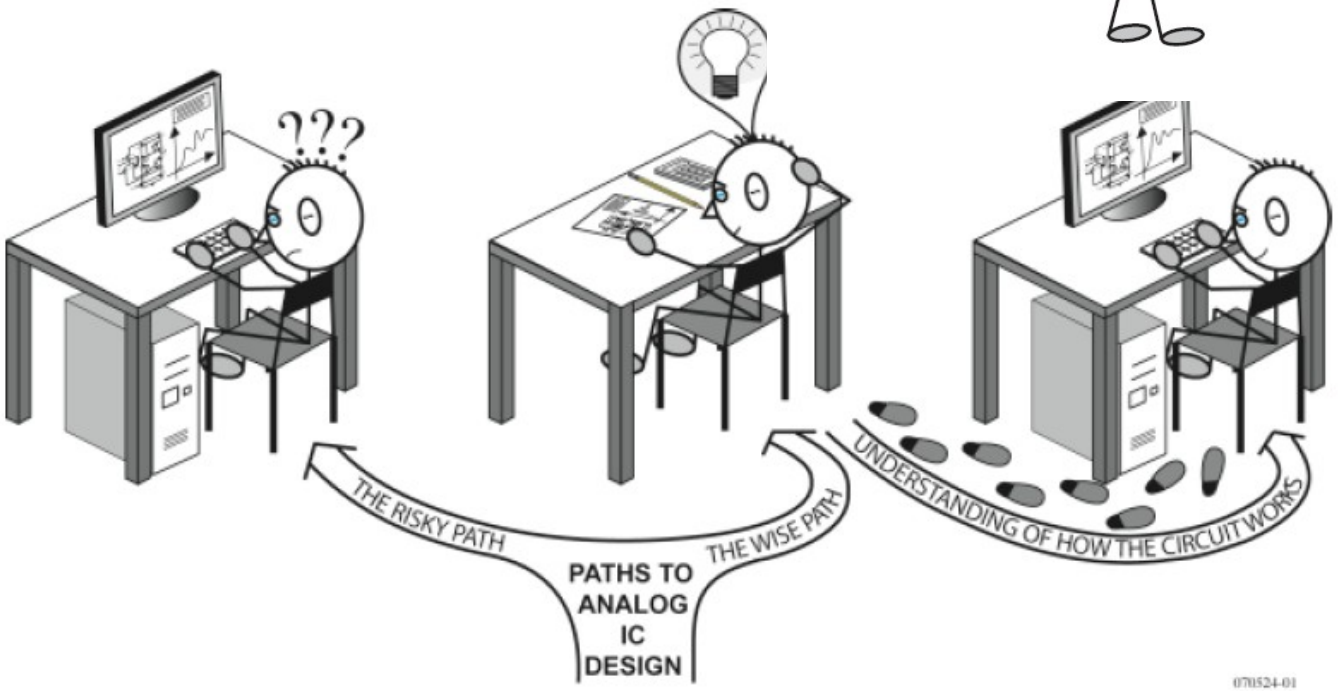
Projektor (Stepper)

http://www.ami.ac.uk/courses/



- IC Design Software (z.B. Cadence)
- Analog- und Digital-Design-Flow
- Spezifikationen
- Systemkonzept
- Schaltungstechnische Realisierung
- Wichtig (P.E. Allen):
- zuerst Schaltung verstehen
- und danach sich vorm PC setzten





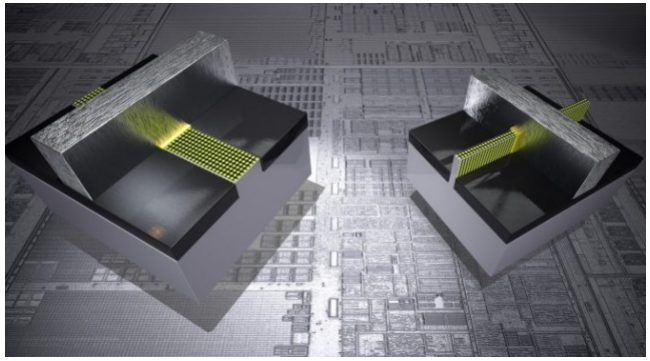
- Chiphersteller wählen („foundry“)

AMS

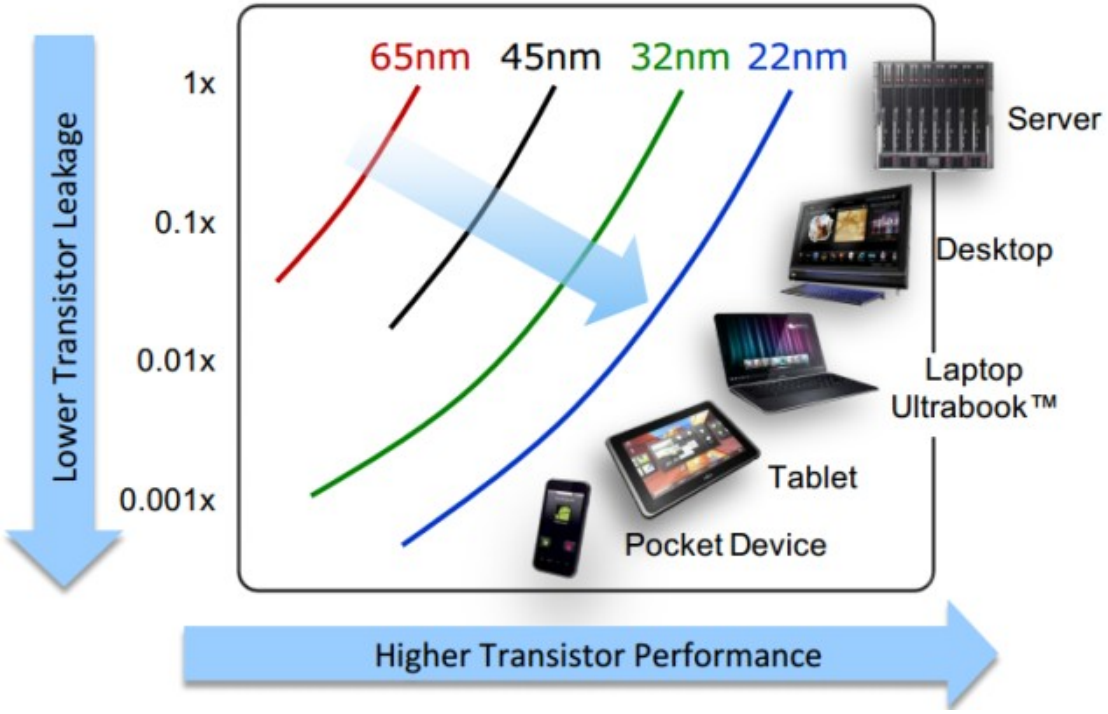
TSMC

UMC

- Prozess wählen
- CMOS (digital, opto, analog, RF)
- Prozesse:
- SOI, BiCMOS, HVCMOS, FINFET, FD SOI
- Process nodes:
- 0.35 um, 0.18um, 0.13um, 90nm, 65nm, 40nm, 28nm…
- Kleinere Prozesse – analog Design schwieriger
- Europractice: Multi Project Runs

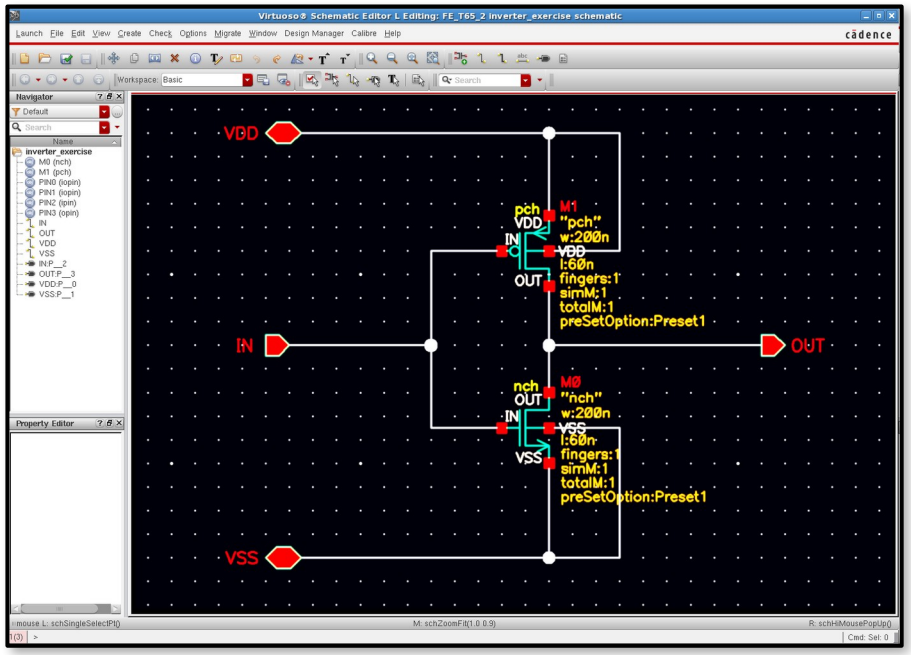


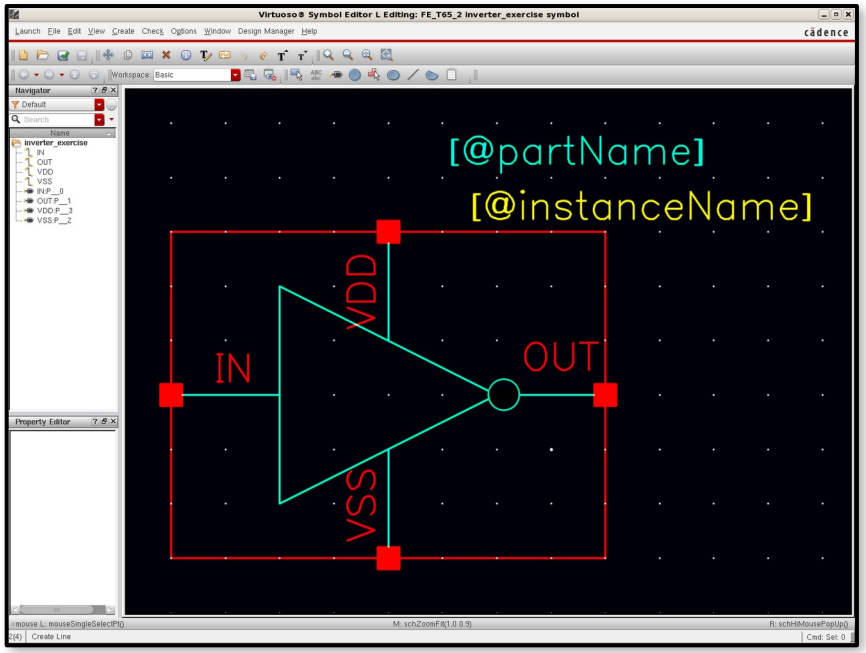
http://www.extremetech.com/



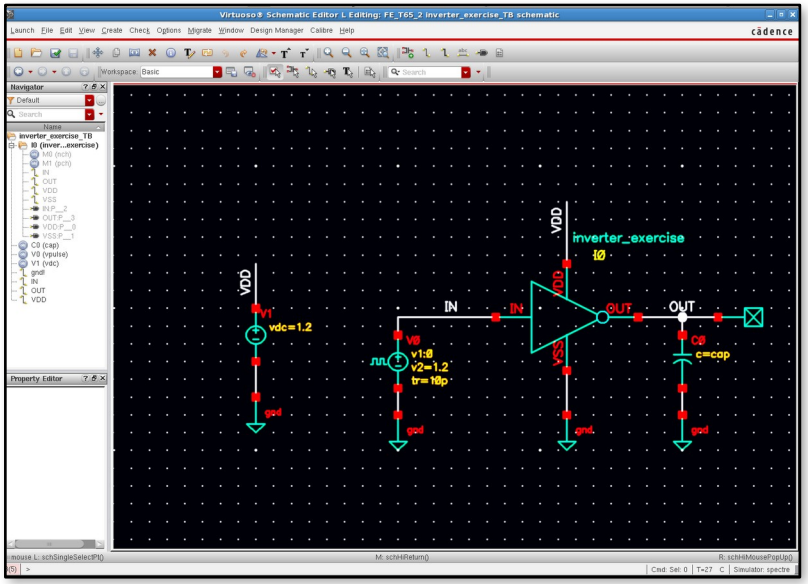
- Simulationsmodelle
- Layout-Regeln
- Process Design Kit (PDK) – Prozess-Bibliothek
- http://www.europractice-ic.com/

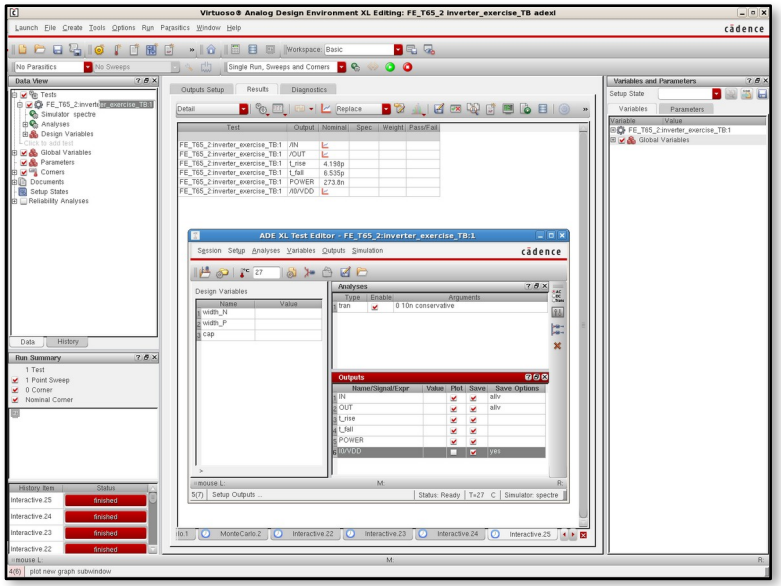
- Schaltplanentwurf im Schematics Editor
- Transistor, Hierarchie, Inputs/Outputs
- Symbol wird generiert – hierarchische Designs

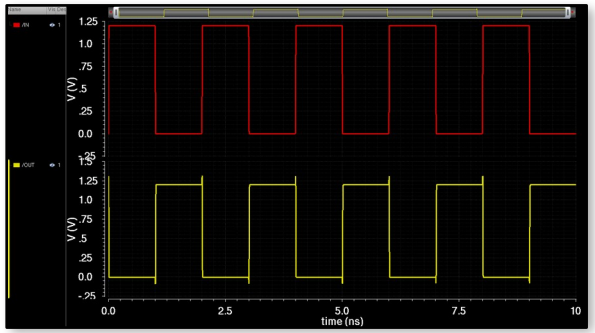




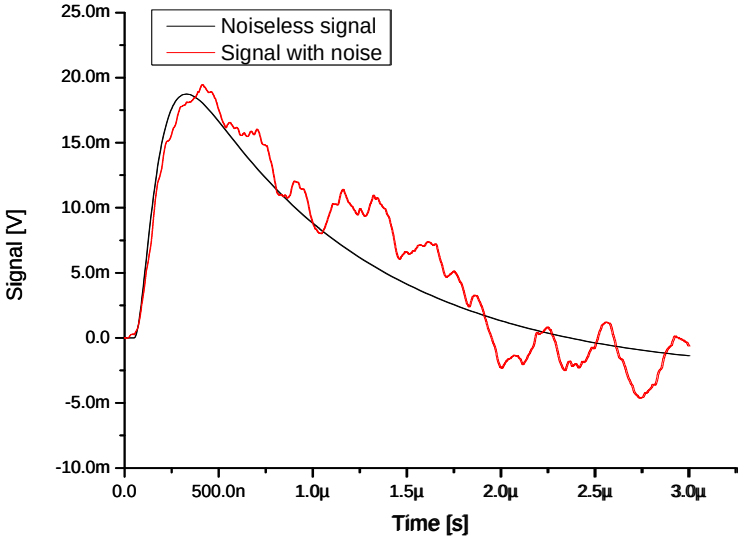
- Schaltung wird simuliert
- Analoge, mixed-mode- oder digitale Simulation
- AC, DC, Großsignale (Transient Analysis)

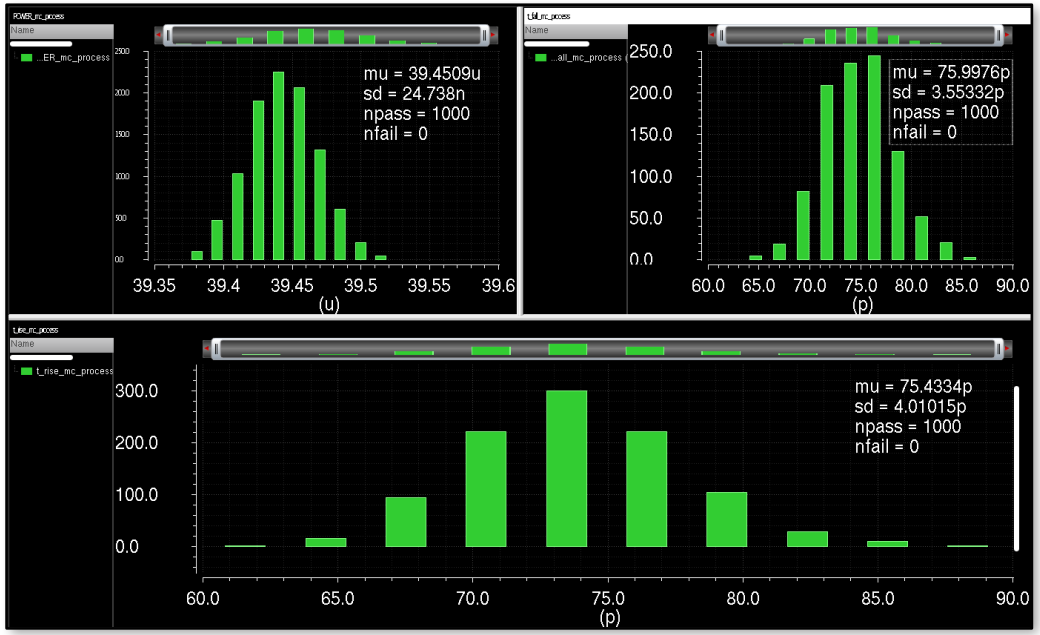




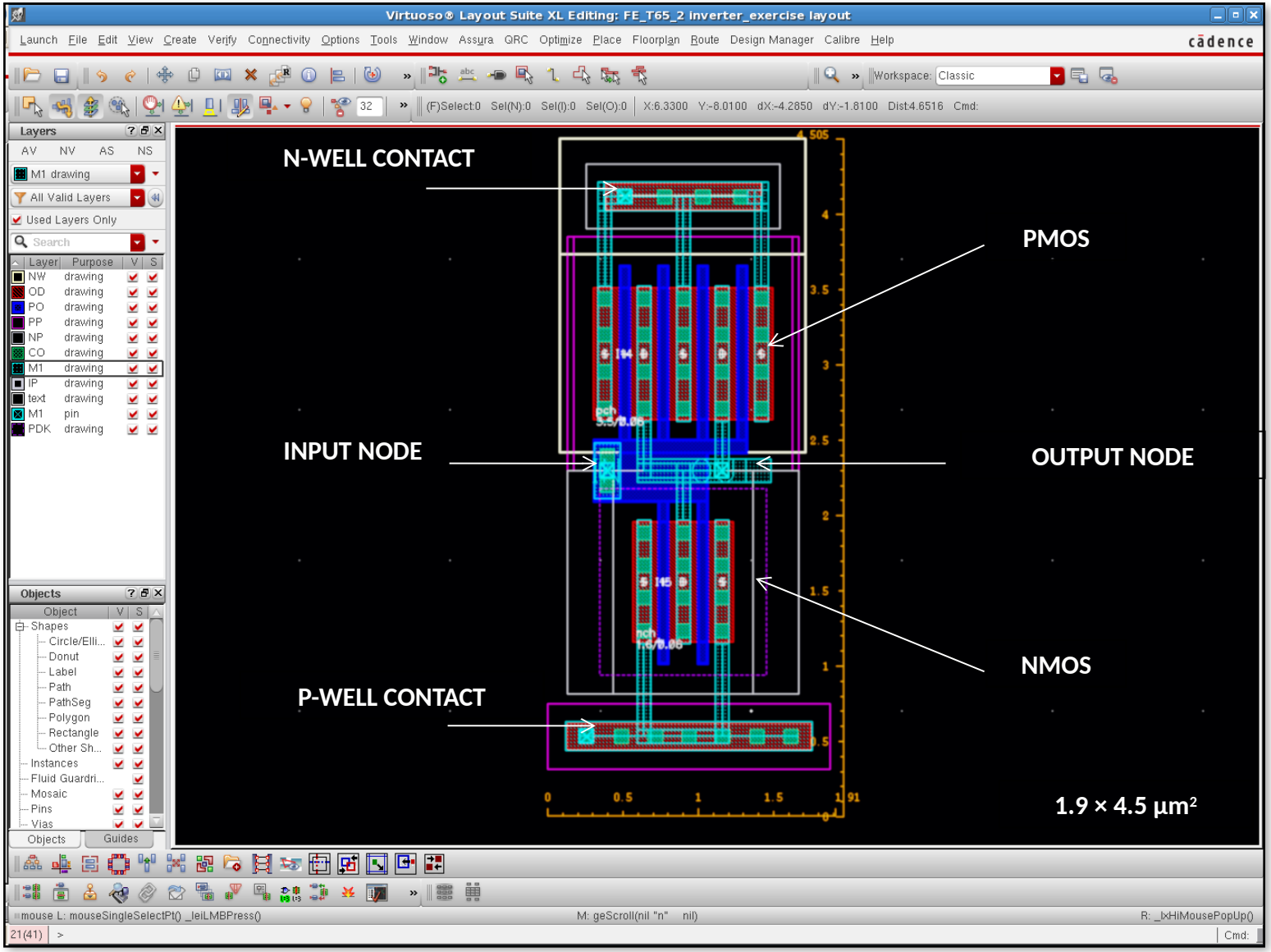


- Rauschen
- Mismatch

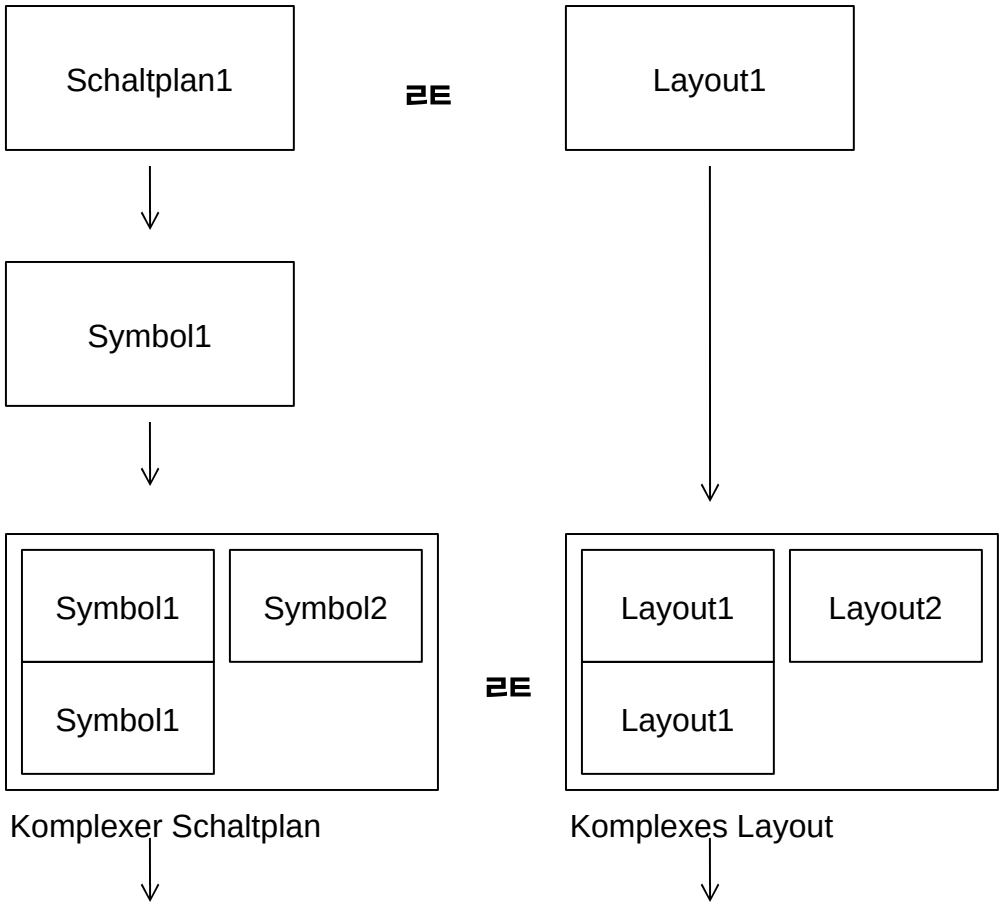




- Layout-Design
- Masken
- Transistoren „von oben“
- Analog Design – Full-Custom Layout (Hand-Layouted)

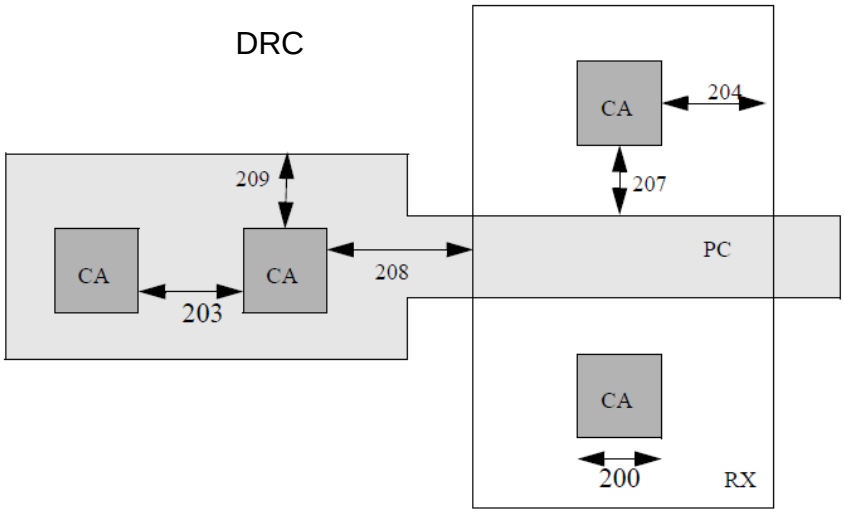

Virtuoso® Layout Suite XL Editing: FE_T65_2 inverter_exercise layout
N-WELL CONTACT
PMOS
INPUT NODE
OUTPUT NODE
NMOS
P-WELL CONTACT
1.9 × 4.5 µm²

- Layout-Editor
- Polygone, Pfade
- Zellen, Blöcke, Hierarchie
- Semiautomatische Generierung von Layouts aus dem Schaltplan ist möglich

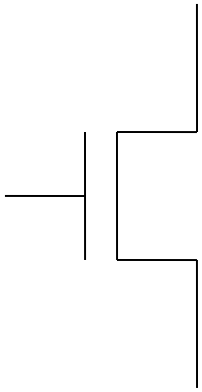


- Layout-Regeln (Teil vom PDK)
- DRC Überprüfung von Layout-Regeln
- LVS Layout Schaltplan Vergleich
- Layout -> Netzliste <-> Netzliste <- Schaltplan
- Extraktion von Kapazitäten aus Layout
- Post-Layout Simulation
- Evt. Anpassung vom Schaltplan notwendig

DRC

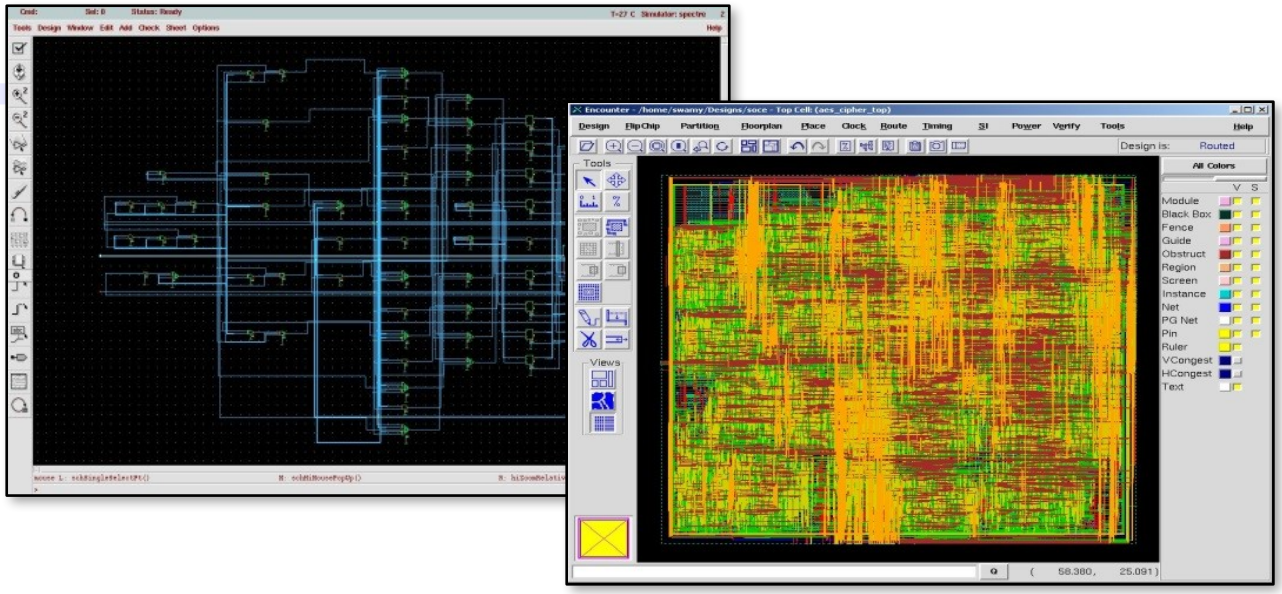


LVS

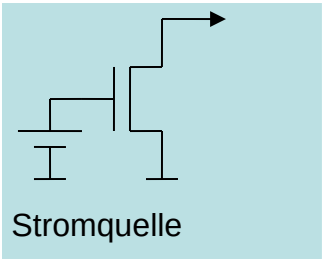


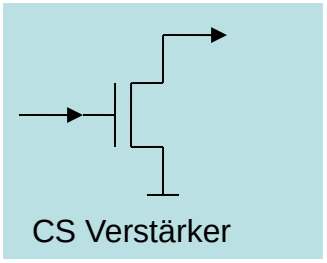
- Digitaldesign
- HDL Code, Simulation -> RTL Code (Schaltplan mit Logikzellen und Registern), Simulation (automatisch) -> Layout, Simulation (automatisch) -> DRC, LVS

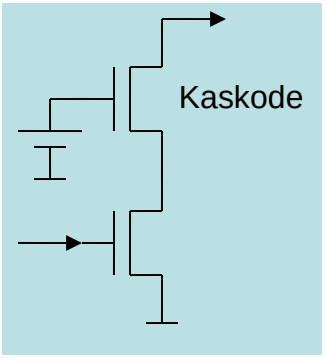
```
19  localparam  IDCODE          = 4'b0010;
20  localparam  INIT_IR_VALUE   = 4'b0101;
21
22
23  reg [IR_LENGTH-1:0]  jtag_ir;           // Instruction register.
24
25  always @ (posedge tck or posedge trst)
26  begin
27    if (trst) begin
28      jtag_ir[IR_LENGTH-1:0]  <= {IR_LENGTH{1'b0}}; // Why not set to IDCODE ??? TODO
29      latched_jtag_ir         <= IDCODE;   // IDCODE selected after reset
30    end else if (state_capture_ir)
31      jtag_ir <= INIT_IR_VALUE;           // This value is fixed for easier fault detection ???
        moved
32    else if (state_shift_ir)
33      jtag_ir[IR_LENGTH-1:0] <= {tdi, jtag_ir[IR_LENGTH-1:1]};
34    else if (state_update_ir)
35      latched_jtag_ir <= jtag_ir;
36  end
37
38  always @ (negedge tck)
39  begin
40    serout <= jtag_ir[0];
41  end
```

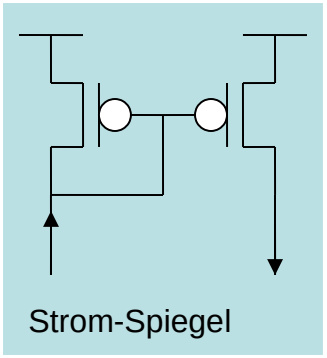


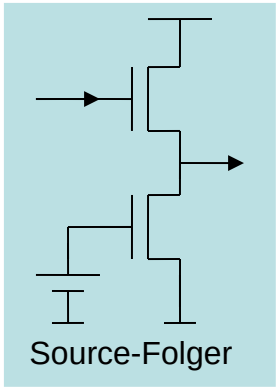
- Schaltungsentwurf
- Tricks:
- Gute Strukturierung
- Verwendung von Grundschaltungen
- Bausteinprinzip

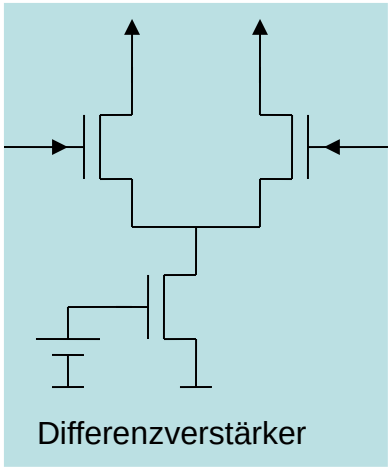




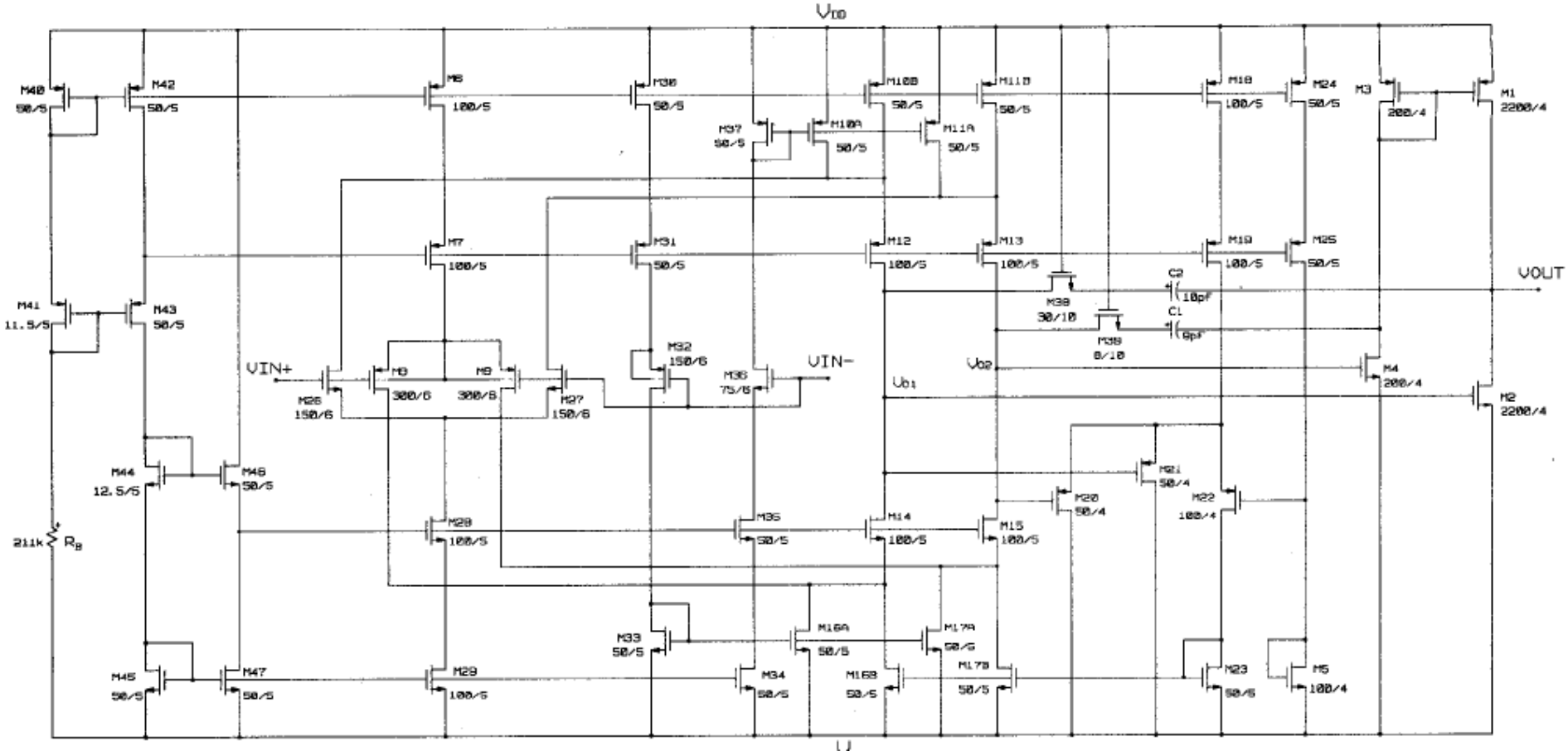








- Verwendung von Grundschaltungen

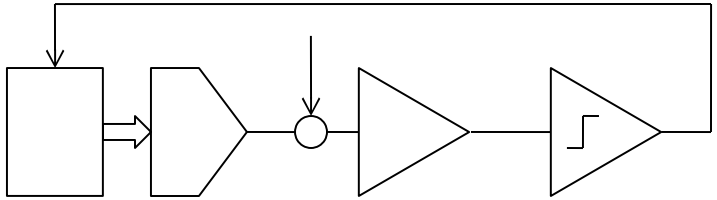


Rail to rail CMOS Opamp: IEEE Journal of Solid-State Circuits, vol. 23, pp. 1414 – 1417, December 1988

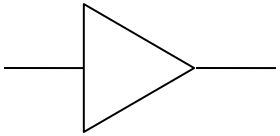
- Hierarchie im Chip

Chip (Integrierte Schaltung)

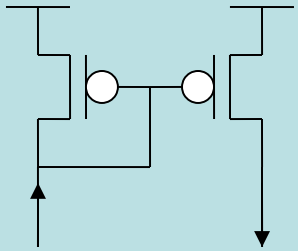
Systeme



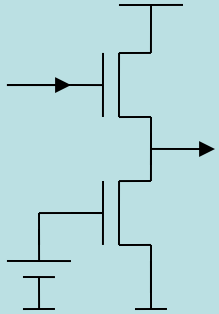
Schaltungen



Grundschaltungen

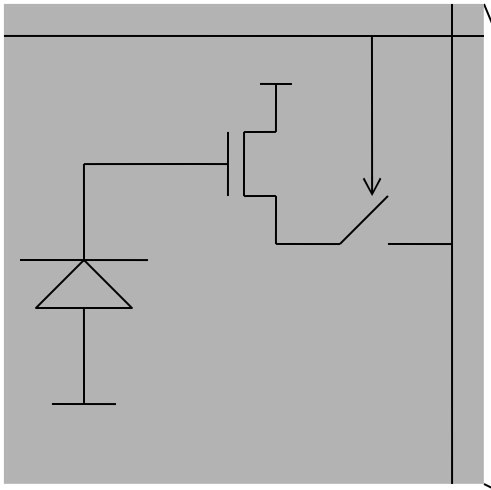


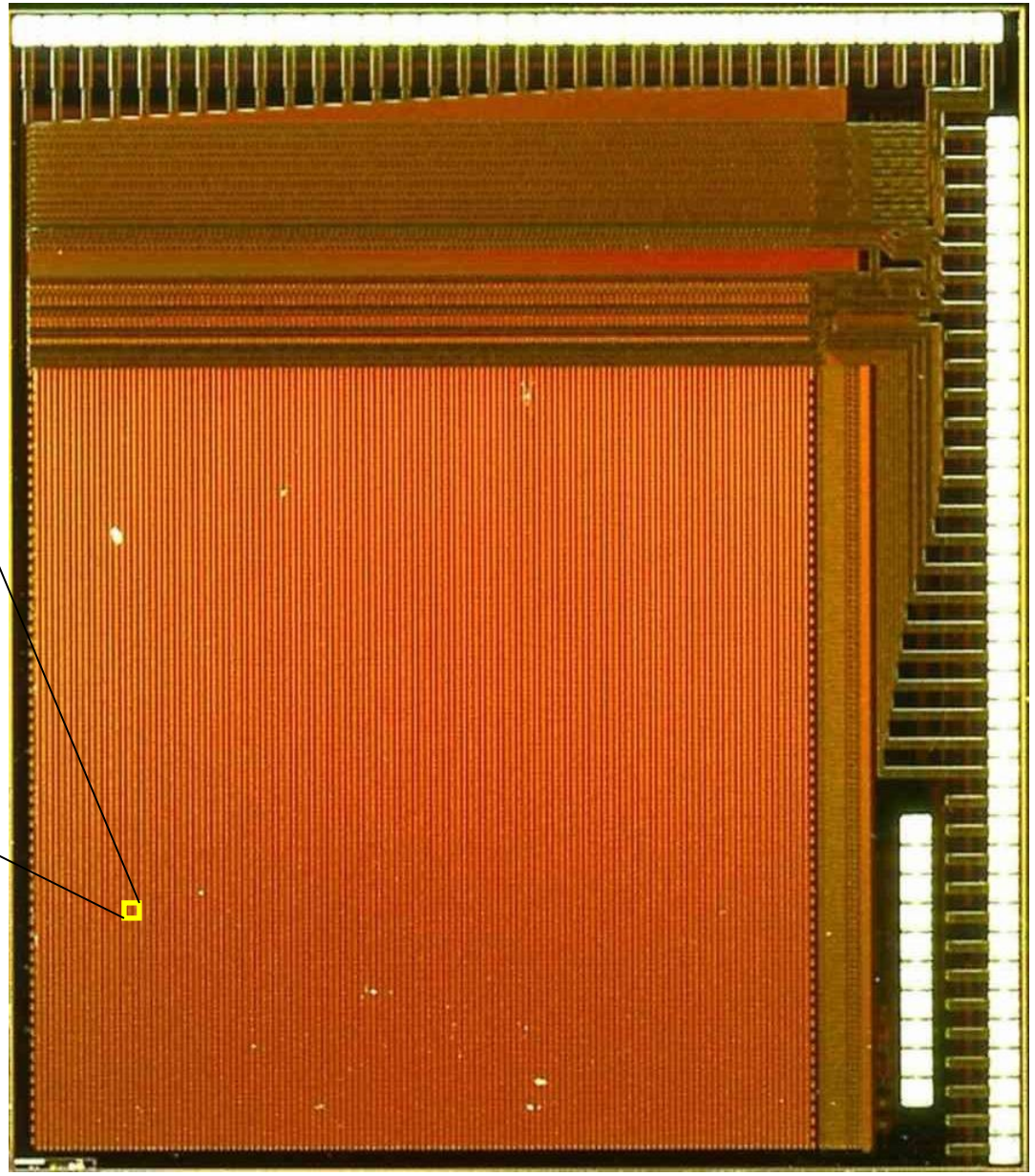
Strom-Spiegel



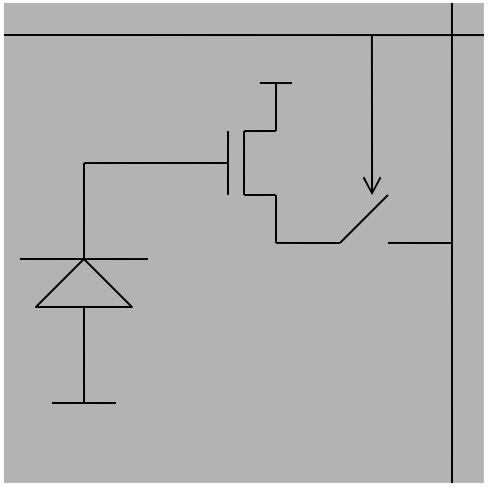
Source-Folger

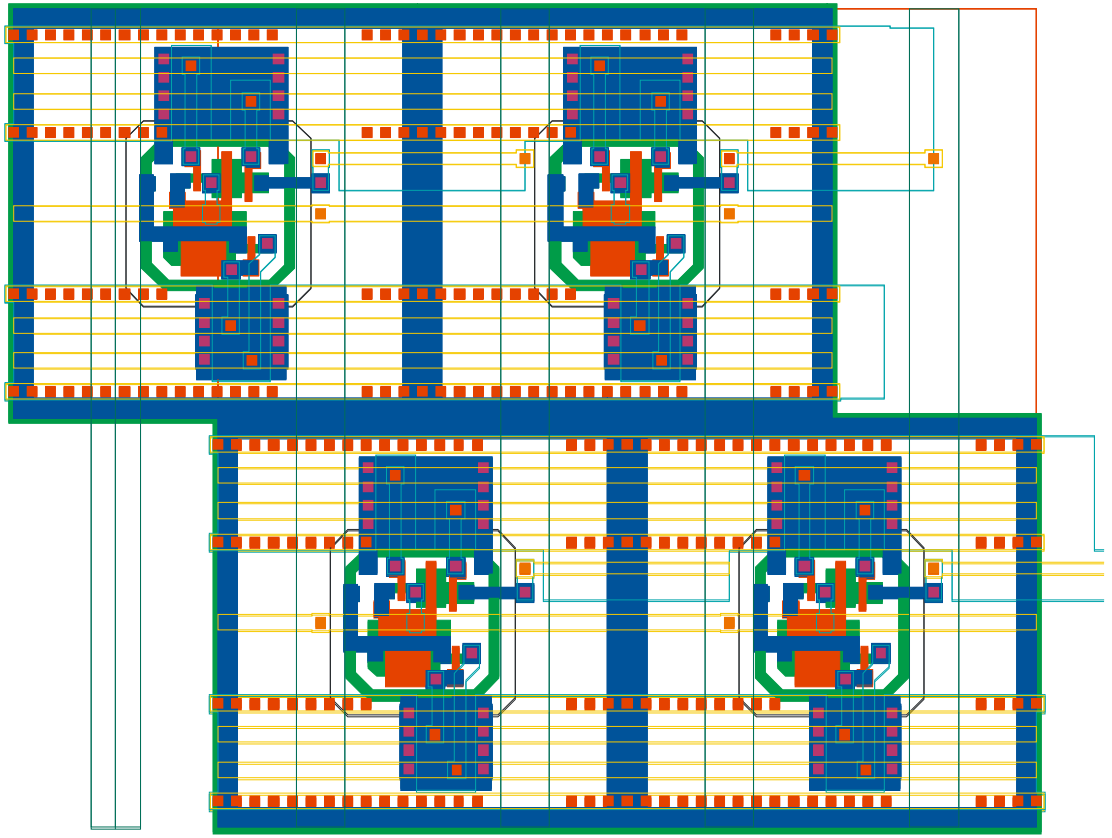
- Pixelsensor
- Pixel:
- Diode, Sensor
- Sourcefolger, Verstärker



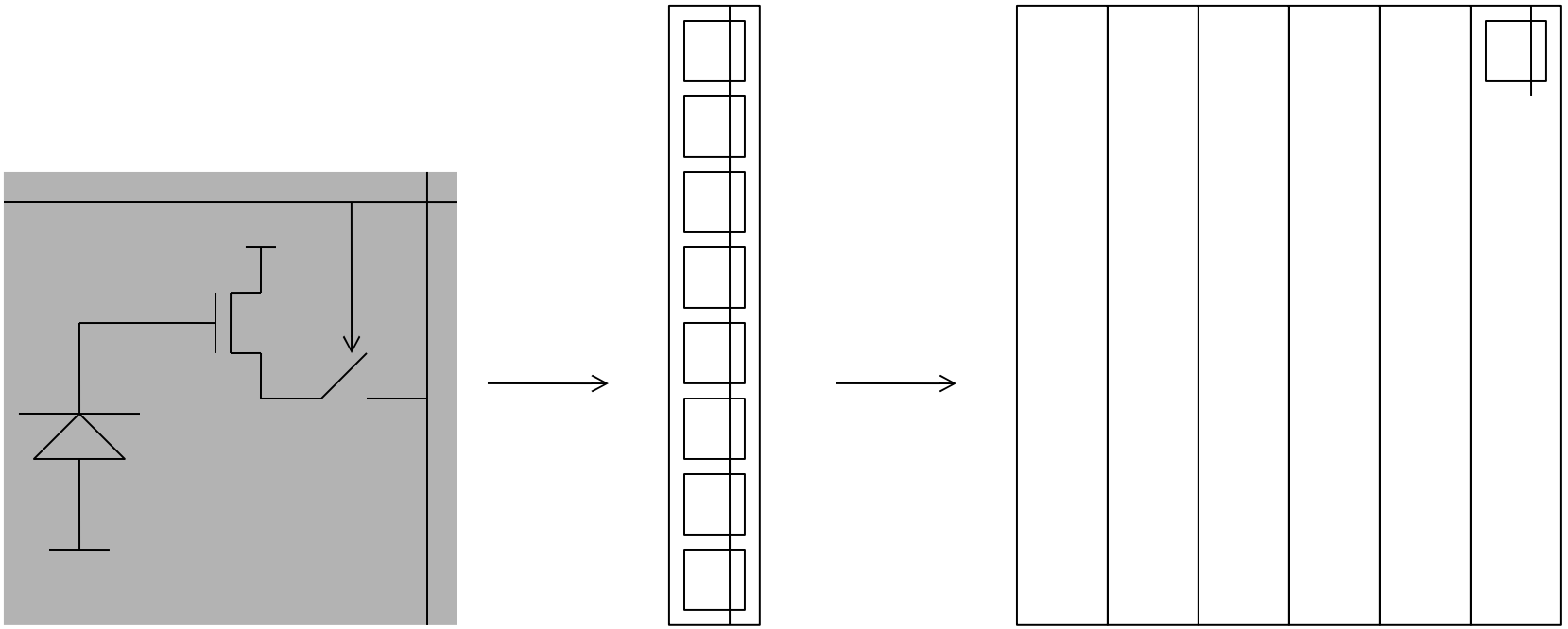


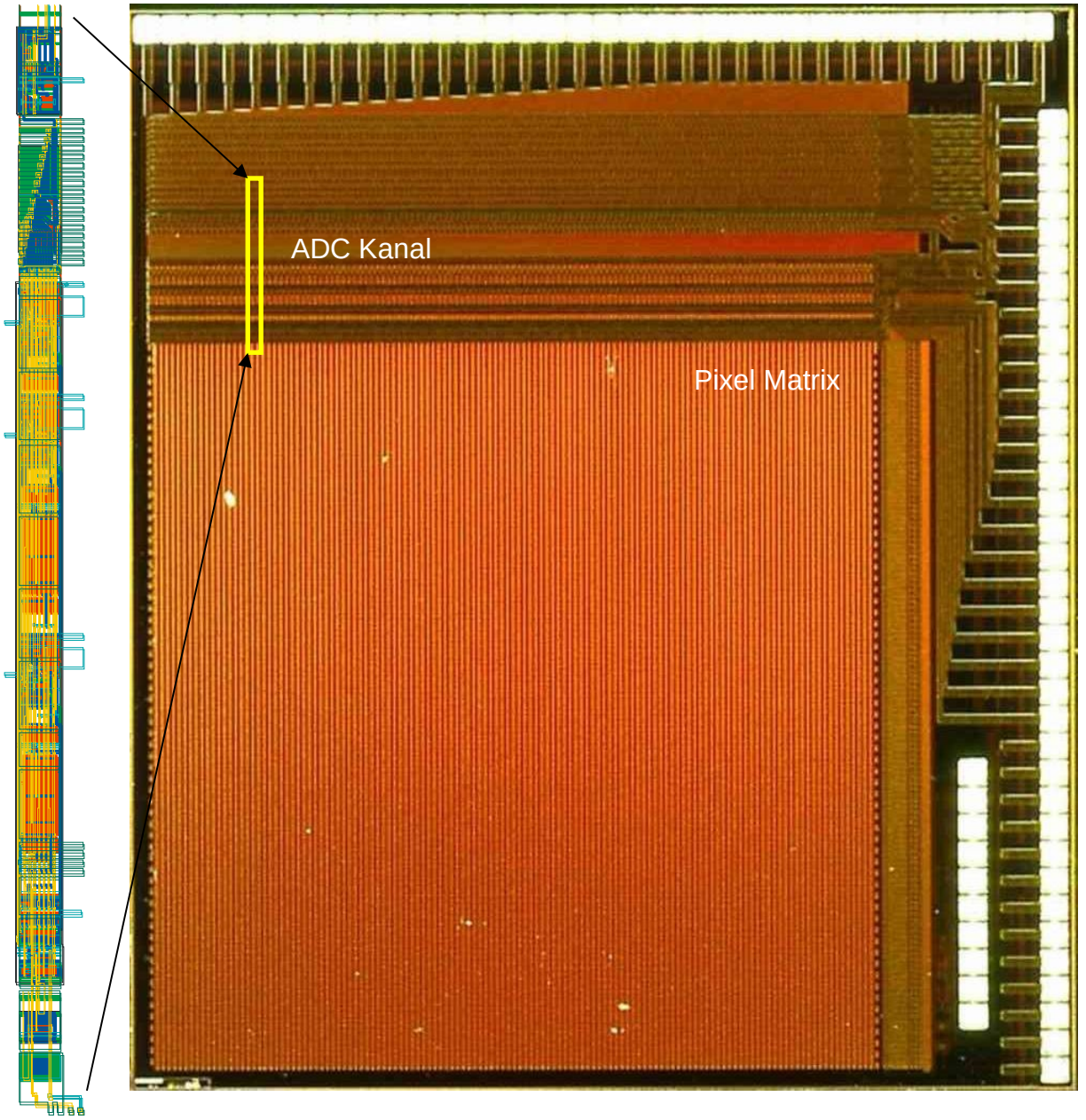
- Pixel Schaltplan
- Pixel Layout
- DRC, LVS



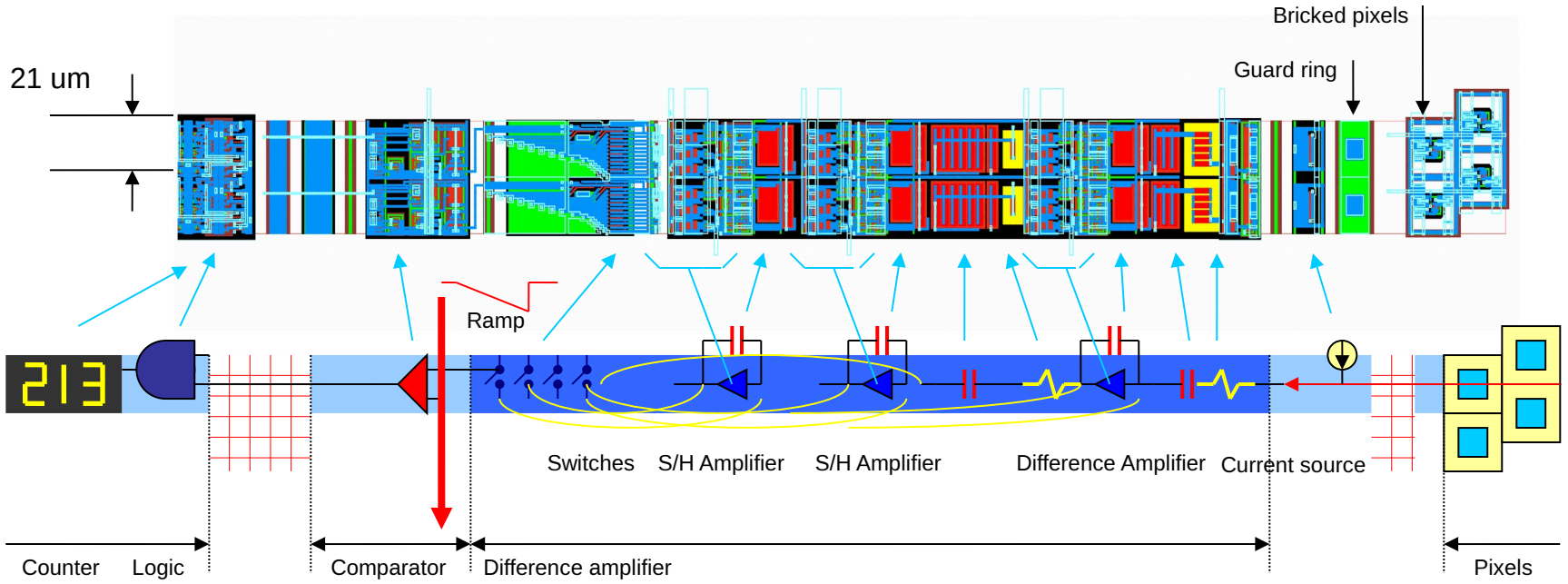


- Pixel
- Pixel Spalte
- Pixel Matrix

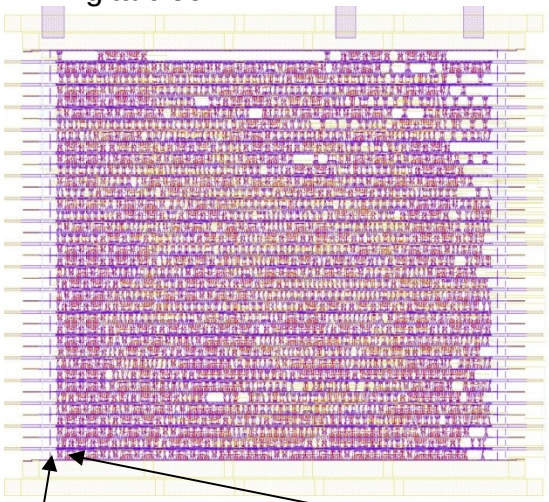


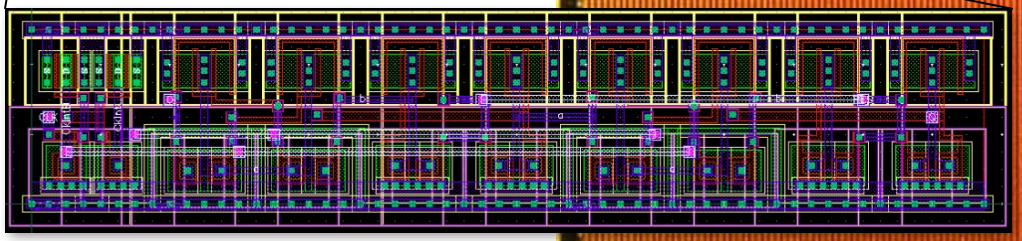

ADC Kanal
Pixel Matrix

- ADC

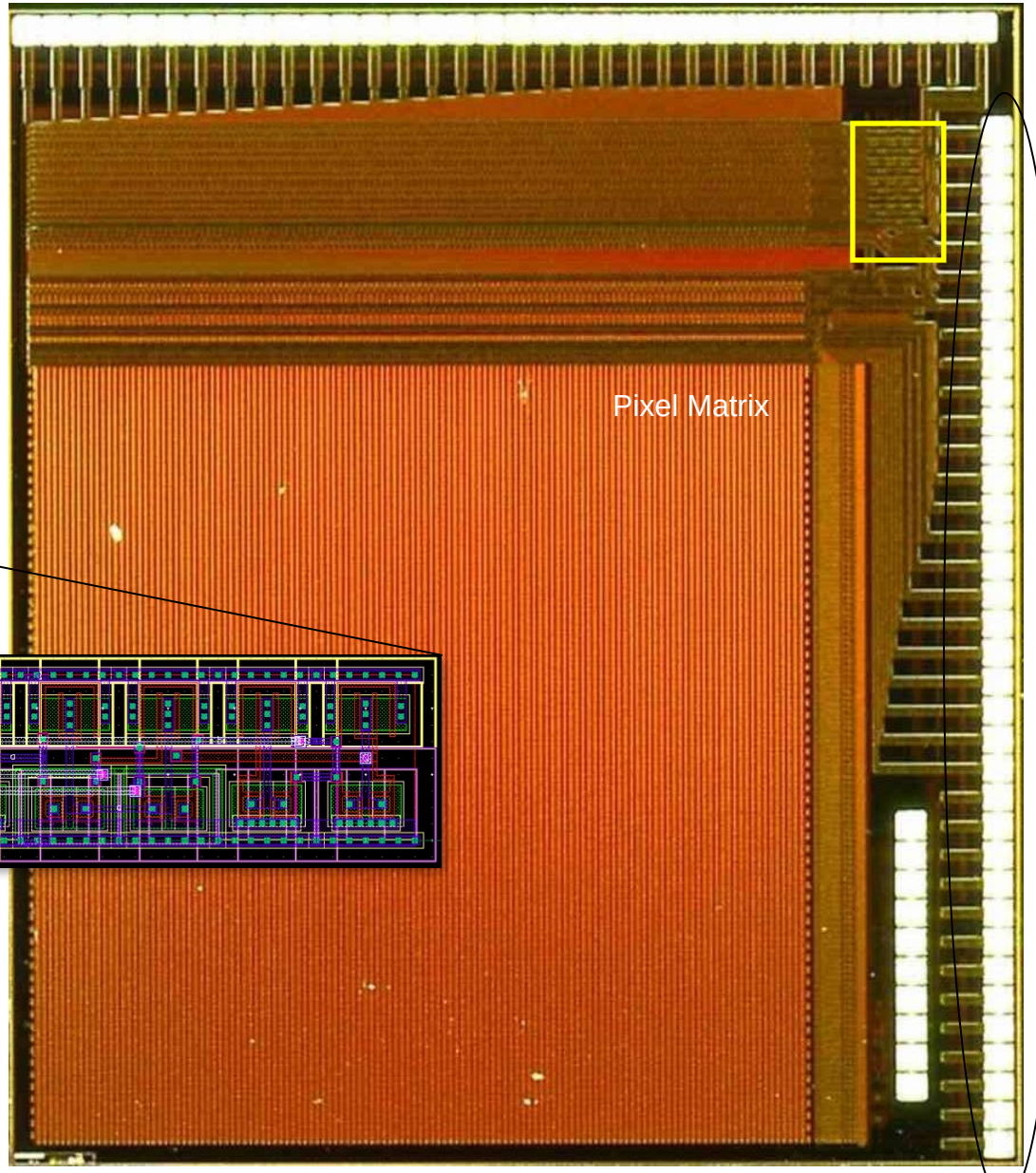

Bricked pixels
Guard ring
21 um
213
Ramp
Switches
S/H Amplifier
S/H Amplifier
Difference Amplifier
Current source
Counter
Logic
Comparator
Difference amplifier
Pixels

Digitalblock

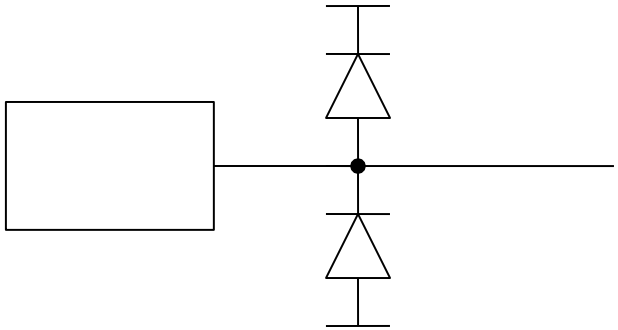


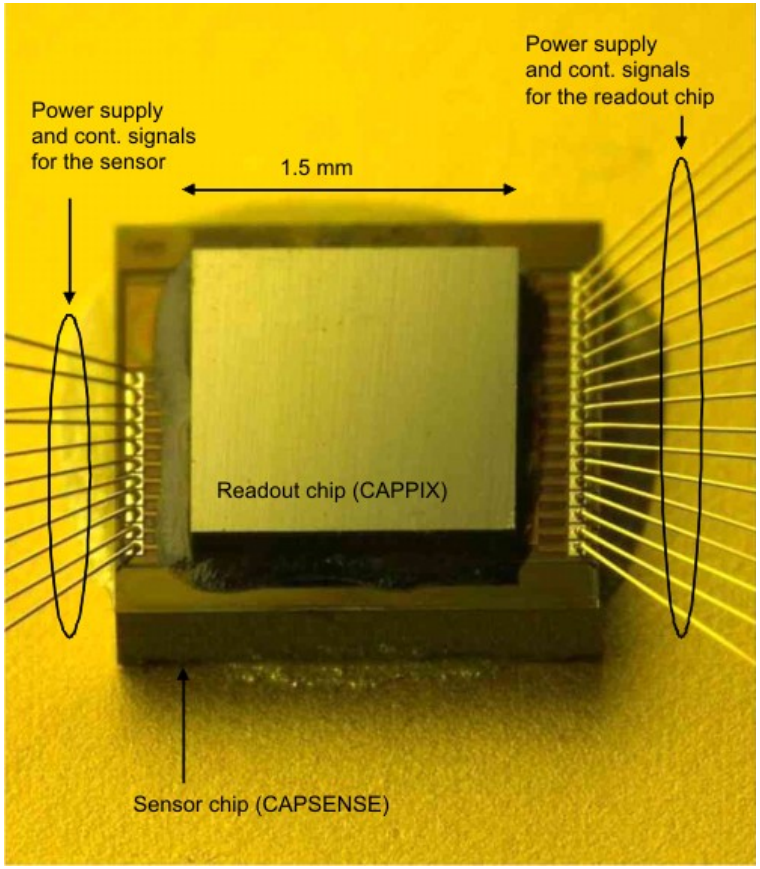


Logik-Zelle (Standardzelle)



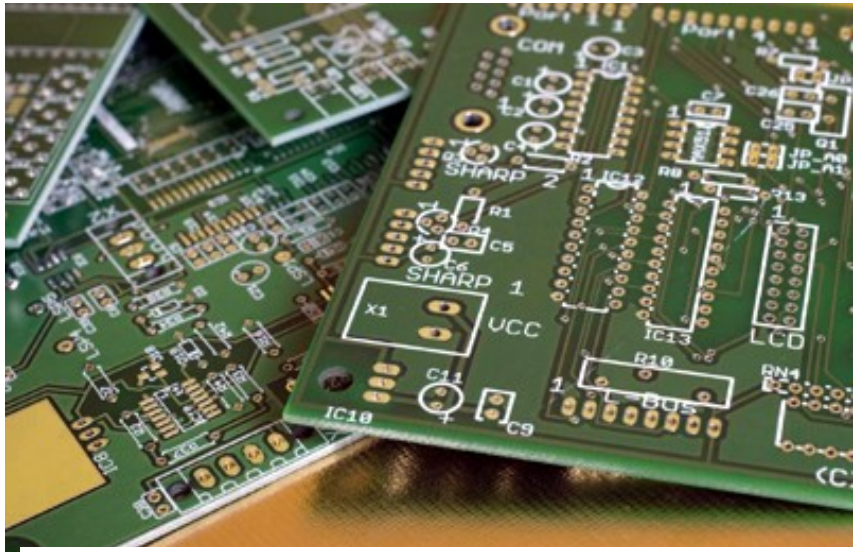
- IO Pads
- Drahtbonden
- ESD protection (ESD Schutz)





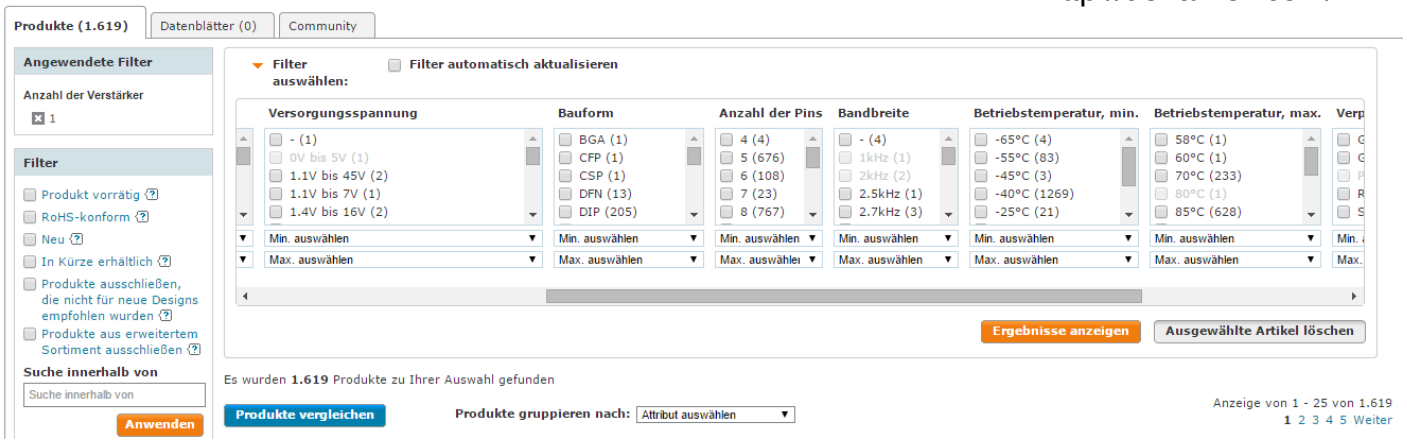
- Design analoger Schaltungen
- Techniken:
- Gegenkopplung
- AC, DC Analyse
- Stabilitätskriterien

- Leiterplatten-Design
- Viele kommerziellen Komponenten



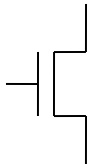
http://www.pcb-pool.com/

http://de.farnell.com/



- IC-Design
- Nur zwei Grundkomponenten
- MOSFET als Verstärker, Stromquelle, Widerstand, Kondensator, Schalter, Diode verwendet
- Komplizierte MOSFET Modelle

- Komplizierte MOSFET Modelle



```
* SUBCIRCUIT SCHEMATIC:
*
*                                drain
*                                  o
*                                  |
*                                  |   Ddb (Includes internal
*                                  |   FET drain area and STI
*                        |   bounded perimeter)
*                        |
*                        |_____|/|_________
*                    d   |     |\|         |
*                        |------\/\/\/-------o
*                        |     rddb         |
*                              |_____|                |
*                    g1    | |                    b1 |            bulk
```

B.1.6 Drain Current Expression

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2v_t)}\right)V_{dseff}}{L_{eff}\left[1 + V_{dseff} / (E_{sat}L_{eff})\right]}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\,litl}(V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{roul}(1 + P_{DIBLCB}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right)$$

```
177  * Core Parameters
178  ******************************
179  + a11 = -0.028
180  + a1o = 22.22
181  + a1w = 0.1
182  + a2o = 18.9
183  + a3l = -0.085
184  + a3o = 1.016
185  + a3w = 0.01
186  + a4l = 0.005
187  + a4o = 0.0155
188  + a4w = -1
189  + agidlw = 0.0
190  + alp1l1 = 0.0
191  + alp1l2 = 1.1
192  + alp1lexp = 0
193  + alp1w = -0.0
194  + alp2l1 = 0.0
195  + alp2l2 = 0.1
196  + alp2lexp = 1
197  + alp2w = -5
198  + alpl = 0.018
199  + alplexp = 0.
200  + alpw = -0.02
201  + axl = 0.4502
202  + axo = 22.12
203  + betw1 = 0.15
204  + betw2 = -0.0
```

```
284  + stthesatl = -0.0135
285  + stthesatlw = 0.00564
286  + stthesato = 1.231
287  + stthesatw = -0.1331
288  + stvfbl = 0.01
289  + stvfblw = 0.001
290  + stvfbo = 0.0008728
291  + stvfbw = 0.0254
292  + stxcoro = 2
293  + themuo = 2.4
294  + thesatbo = 0.1
295  + thesatgo = 0.2126
296  + thesatlexp = 0.8524
297  + thesatlw = 0.00566
298  + thesato = 0.0108
299  + thesatw = -0.08
300  + tkuo = 0
301  + vfbw = -0.011
302  + vnsubo = 0
303  + vpo = 0.09954
304  + wbet = 2.039E-08
305  + wkuo = 0
306  + wkvtho = 0
307  + wlod = 0
308  + wlodkuo = 0
309  + wlodvth = 0
310  + wseg = 1E-08
311  + wsegp = 5.444E-09
```

- Widerstand und Diode selten benutzt
- Kondensatoren ersetzt Widerstände
- MOSFETs ersetzen Dioden
- Transkonduktor

- Inhalt des Kurses:
- Approximative Methode für Schaltungsanalyse
- Analyse von Schaltungen mit Rückkopplung
- Berechnung von Zeitkonstanten
- Stabilitätskriterien
- Verstärkern
- Komplexere Schaltungen
- Mehrstufige-, differenzielle-, Rail to Rail-Verstärkern, Komparatoren
- Systeme: Switched Capacitor Schaltungen, ADCs
- Jede zweite Woche Übungen mit Chipdesign-Software
- Prüfung – Mündliche Prüfung – Beispiele aus den Übungen

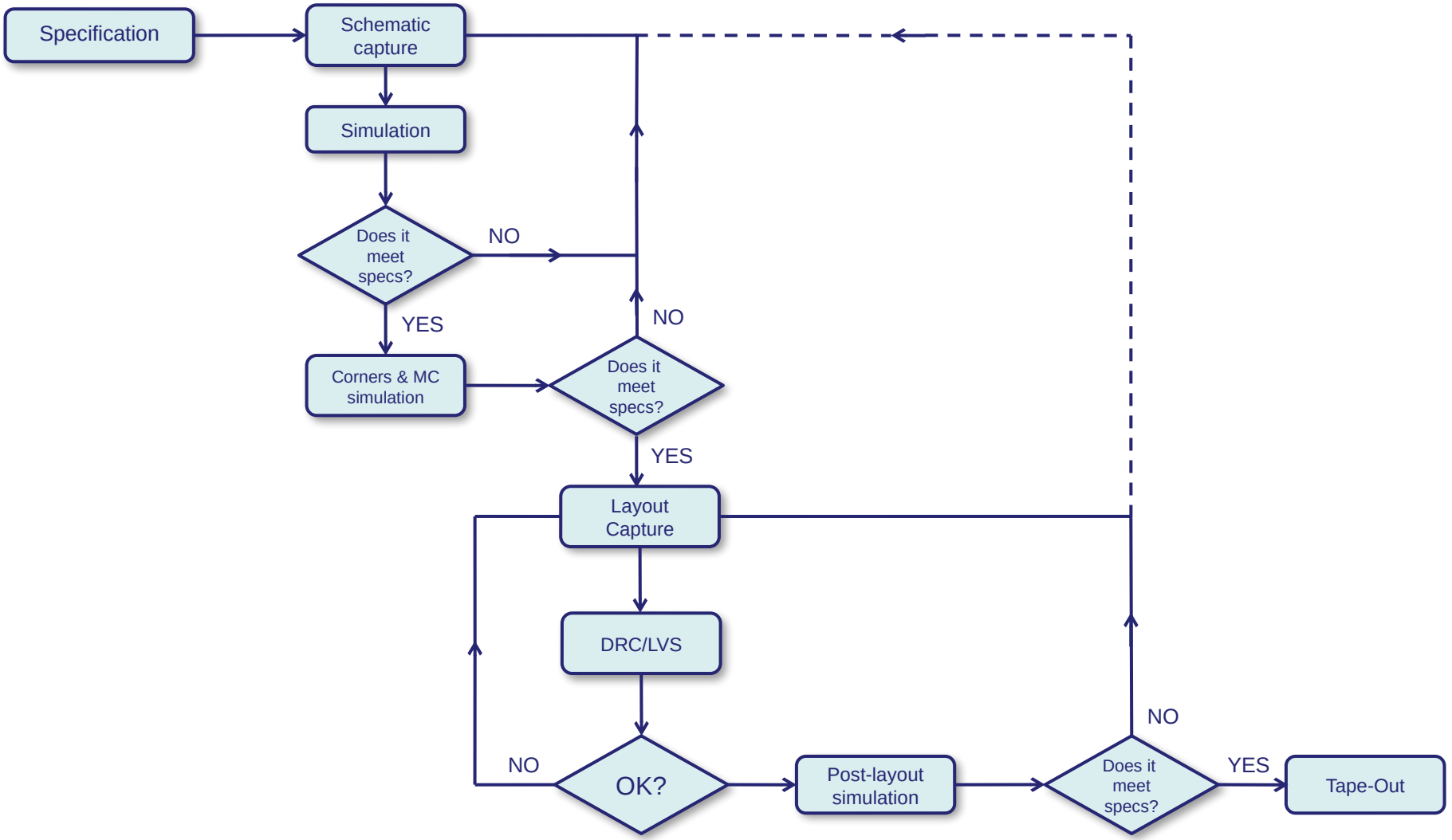
- Literatur
- **Design of Analog CMOS Integrated Circuits** von Behzad Razavi
- **Operation and Modeling of the MOS Transistor,** Yannis Tsividis, Colin McAndrew
- **Analog Integrated Circuit Design**, David A. Jones, Ken Martin, John Wiley & Sons, Inc
- **Analysis and Design of Analog Integrated Circuits**, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, Inc
- **The Art of Analog Layout**, Alan Hastings, Prentice Hall
- **CMOS Analog Circuit Design,** Allen-Holberg, Oxford Press, 1987
- **Analog Design Essentials,** W. Sansen, Kluwer International Series in Engineering and Computer Science
- **Microelectronics** von Jacob Millman von T (1999)

- Themen
- 1 Rückkopplung, Formeln für Schaltungen mit Rückkopplung, Einfluss auf Verstärkung, Zeitkonstanten, Invertierender und Nichtinvertierender Verstärker
- 2 Grundlegende Verstärker-Schaltungen und grundlegende Bauteile: CMOS Verstärker (Common Source), Cascode, Source-Folger
- 3 Halbleiter, Diode, MOSFET (DC, AC, Rauschen, Matching)
- 3ü Bipolar Transistor, MOS-Kondensator, Schwache Inversion, BSIM-Modell
- 4 AC Analyse (Frequenzverhalten der Schaltungen), Übertragungsfunktion für Schaltungen mit Kondensatoren, Bestimmung von dominanten Zeitkonstanten (RC Regel), Methode der Nullimpedanzen
- 4ü Common Source Verstärker
- 4ü Single Ended Verstärker, Kaskaden und Kaskoden
- 5 Einfluss von Rückkopplung auf Zeitkonstanten, Stabilität, Nyquist Regel
- 5ü Transimpedanz Verstärker, Spannungsregler
- 7 Komplexere Verstärker, Einstufig, Zweistufig, Rail to Rail, Volldifferentiell, Klasse AB
- 8 Komparatoren
- 9 Switched Capacitor Schaltungen
- 10 Filter (RC, Gm-C, Switched Capacitive Filter)
- 11 ADCs (Dual und Single Slope, Flash, Subranging, SAR mit Kondensatoren, SAR mit Stromquellen, SAR Asynchron, Sigma Delta, Zyklisch mit Stromzellen, Zyklisch mit Switched Capacitive Schaltungen)
- 12 Spannungsreferenz, PLL und VCO, LVDS Treiber, LVDS Empfänger

- Was haben wir gelernt?
- Es geht um analoges Chipdesign
- Chipdesignsoftware Cadence – Übungen
- Analoges Designflow: Schaltungsentwurf, Simulation (AC, DC, Transiente Simulation, Rauschen, Matching), Layoutentwurf, DRC, LVS
- Digitales Designflow: HDL Code, Simulation -> (automatische) RTL Synthese, Simulation (Standard-Logikzellen) -> Layout-Synthese, Simulation
- Am Anfang des Projekts muss man Hersteller (foundry, vendor) und Technologie wählen, PDK (Process Design Kit) (Technologiespezifische Bibliotheken fürs Cadence) besorgen
- Europractice
- Transistorherstellung siehe Link
- Chipprojekte sind hierarchisch aufgebaut
- Grundbausteine: Common Source, Cascode, Source Follower, Current Mirror, Differenzpaar
- Widerstände selten benutzt – Alternative ist C
- Transistormodelle sind sehr komplex – BSIM Model
- Fragen
- Welche Chiphersteller kennen wir?
- AMS, TSMC, UMC, IBM, GF, LF, XFAB…
- Welche Prozesse?
- CMOS, SOI, HVCMOS, FINFET, BCD, BiCMOS
- Welche „process nodes“: 0.35, 0.24, 0.18, 0.13, 90nm, 65nm, 45nm…
- Das meistbenutzte MOSFET-Modell: BSIM
- Welche Firmen sind fürs Leiterplattendesign nützlich? PCB pool, Farnel

- Vielen Dank für Ihre Aufmerksamkeit

Analog Design Flow



Digital Design Flow