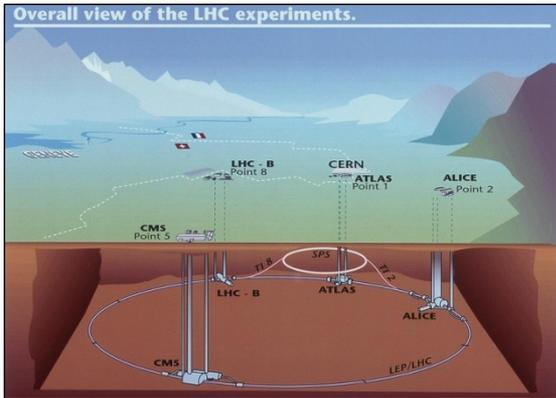


Design analoger Schaltkreise

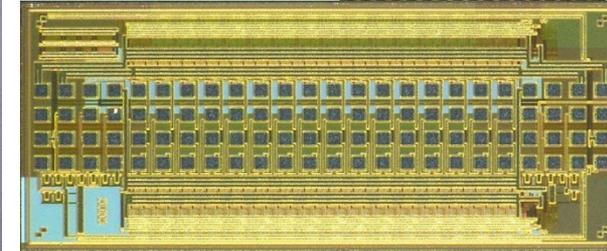
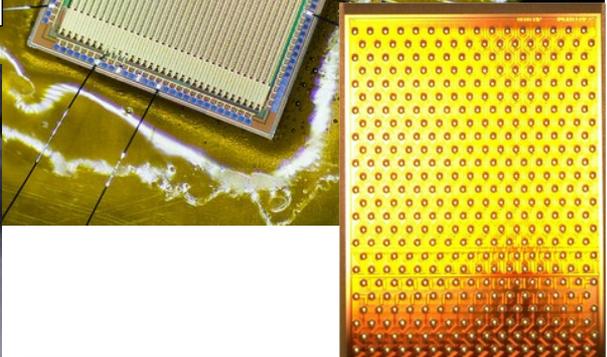
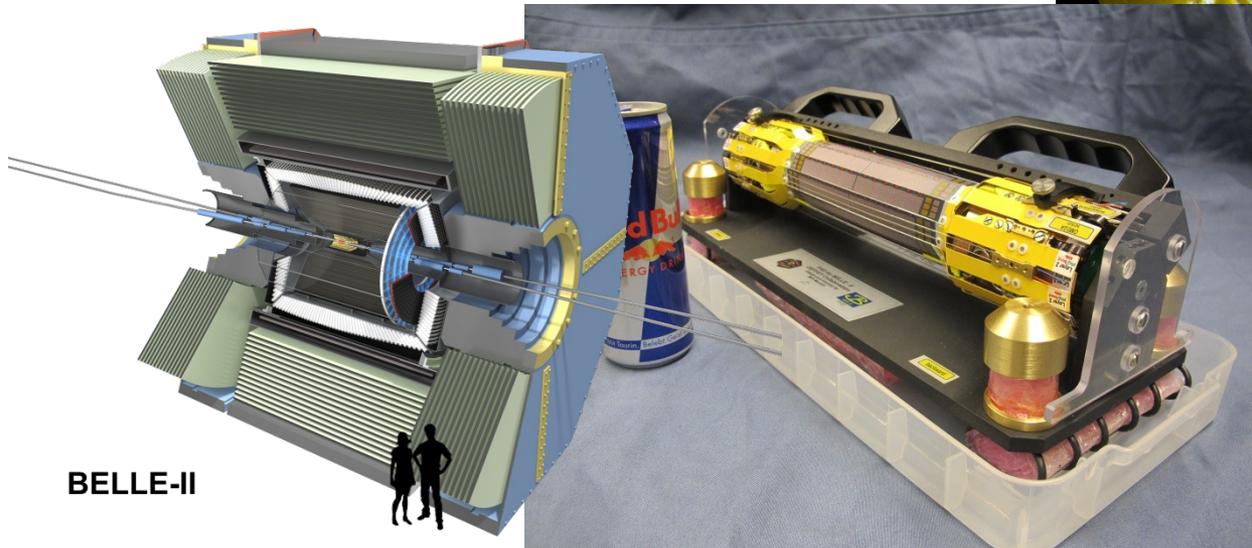
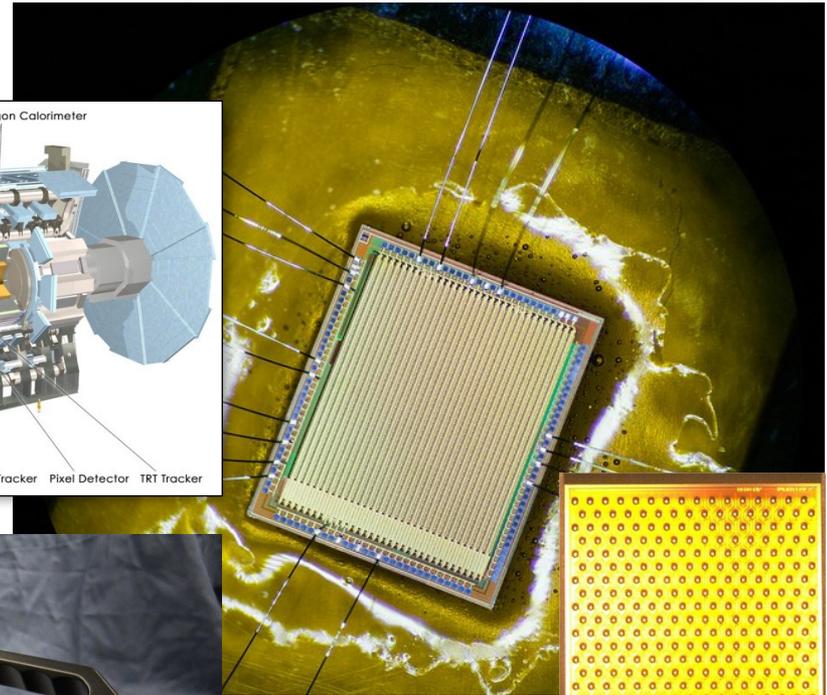
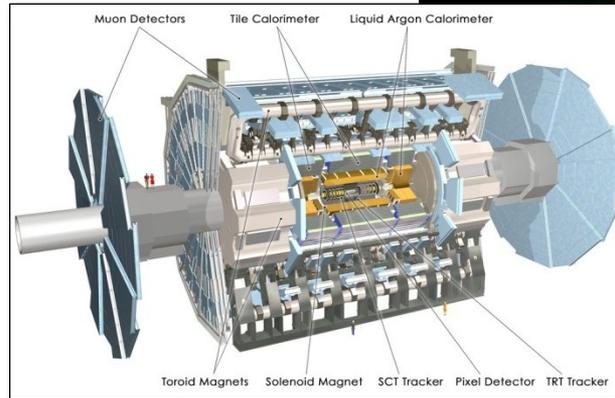
Vorlesung 1

- Institut für Prozessdatenverarbeitung (IPE) am KIT Campus Nord
- ASIC und Detektor Labor
- Detektoren an Teilchenbeschleuniger

Large Hadron Collider



Experiment ATLAS



Design analoger Schaltkreise

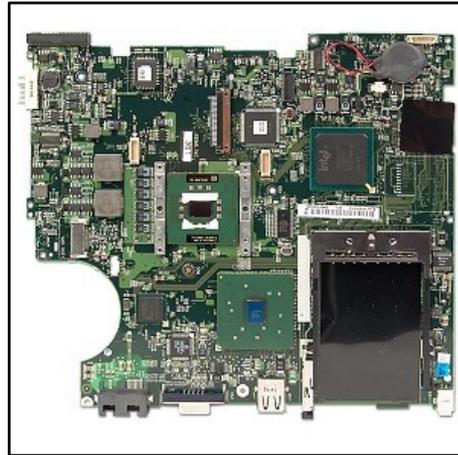
- Vorlesungen und praktische Übungen mit Chipdesign-Software (CIP-Pool am IMS)
- Übungen ab November
- Kontakt: ivan.peric@kit.edu
- Kontakt: richard.leys@kit.edu
- Inhalt ist neu – neue Skripten bald
- https://www.ims.kit.edu/324_201.php

Electronic device

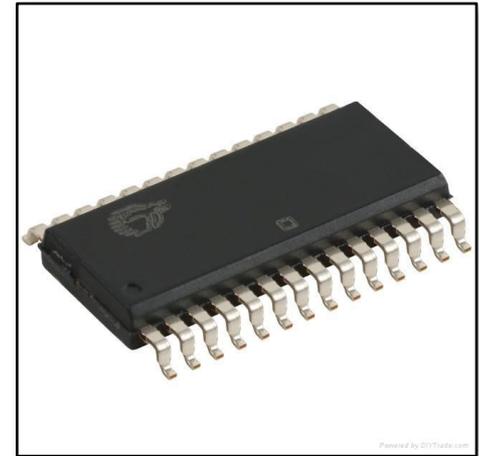


← 30cm →

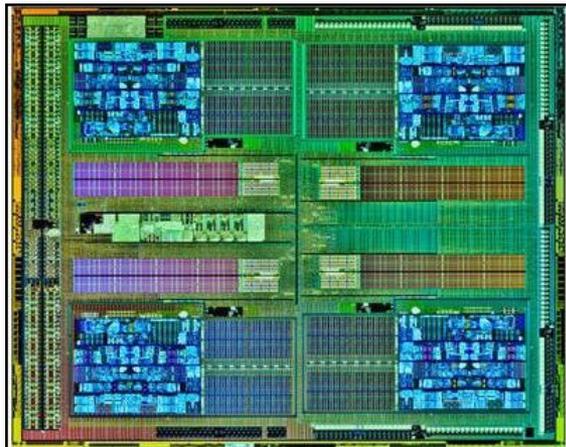
PCB



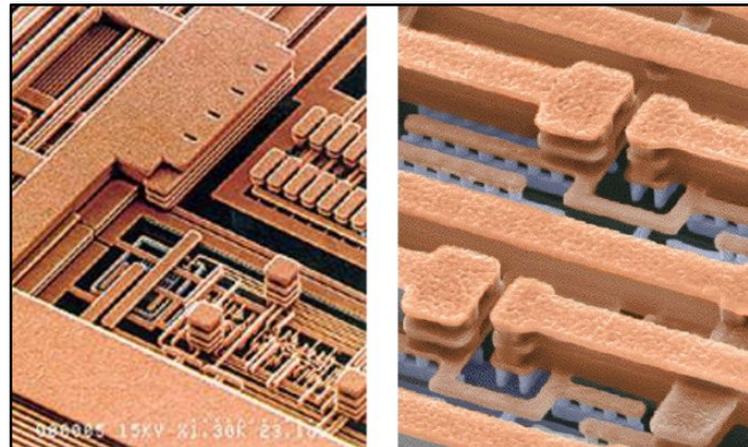
Integrated circuit



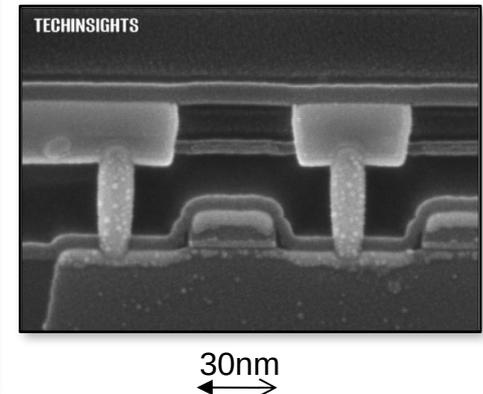
Integrated circuit - core



Interconnection



Transistor



- Vorkenntnisse: Vorlesungen Elektronische Schaltungen und VLSI-Technologie
- MOSFET, JFET, Bipolar-Transistor (BJT)
- Einfache elektronische Schaltungen
- Kleinsignalmodelle, Arbeitspunkt
- Prinzipien der IC Herstellung

- Prinzipien der IC Herstellung
- Wiederholung von Schritten
- Oxid-, Silizium- oder Metalllagen werden auf einem Si-Substrat erzeugt
- Photolithographie (Photolack, UV Licht, trocken- und nassätzen)
- Lagen werden strukturiert
- Silizium wird dotiert
- Link: <http://www.halbleiter.org/wie-wird-ein-mikrochip-hergestellt/>

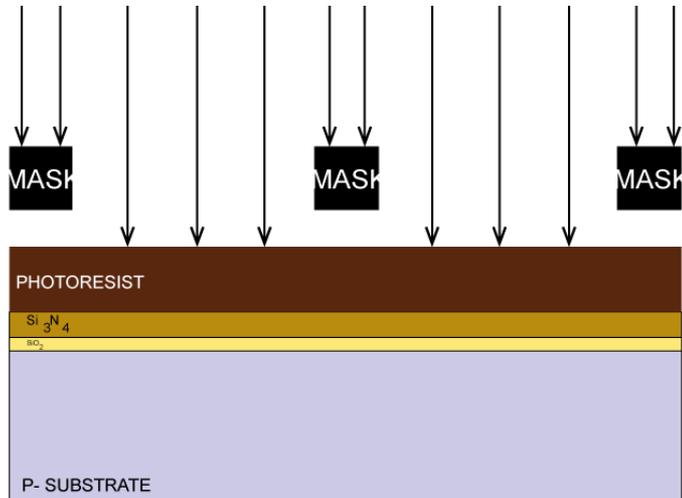
1. Deposition of silicon oxide and nitride



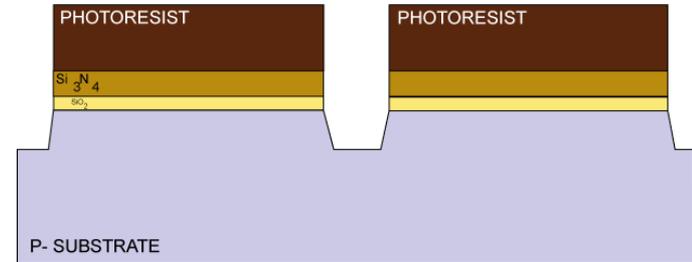
2. Photoresist deposition



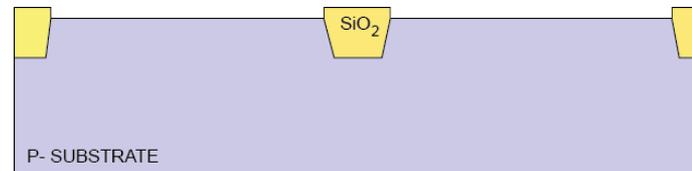
3. Illumination of the photoresist through the mask



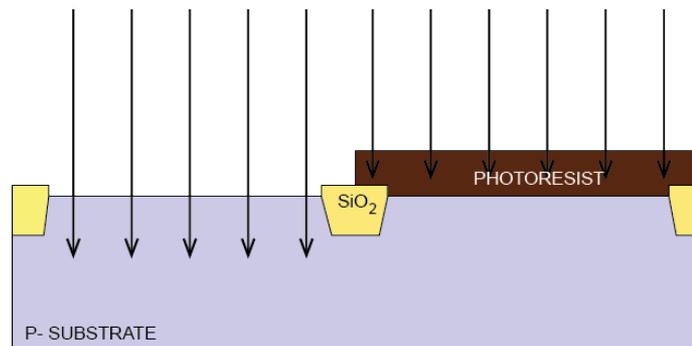
4. Removing illuminated photoresist, etching silicon nitride, etching isolation trenches in silicon



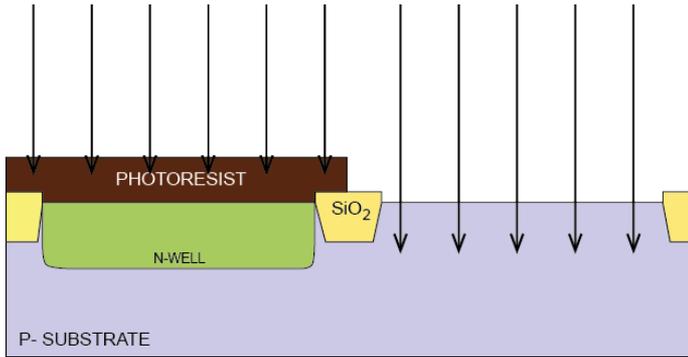
5. Filling isolation trenches with SiO2



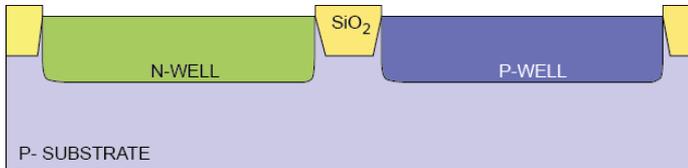
6. Ion implantation (Phosphor ~100 keV) -> N-well formation



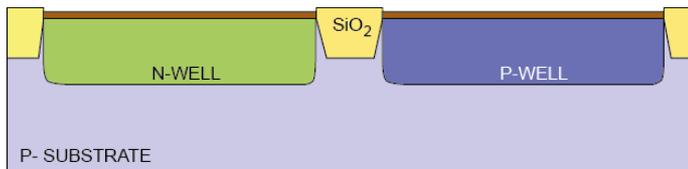
7. Ion implantation (Boron ~100 keV) -> P-well formation



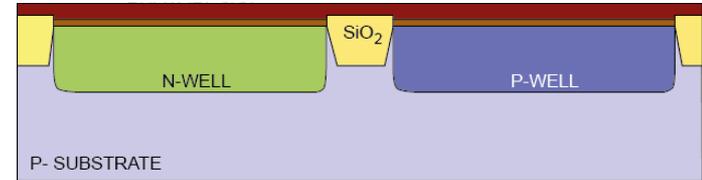
8. N-well and P-well are ready for implementing NMOS and PMOS transistors



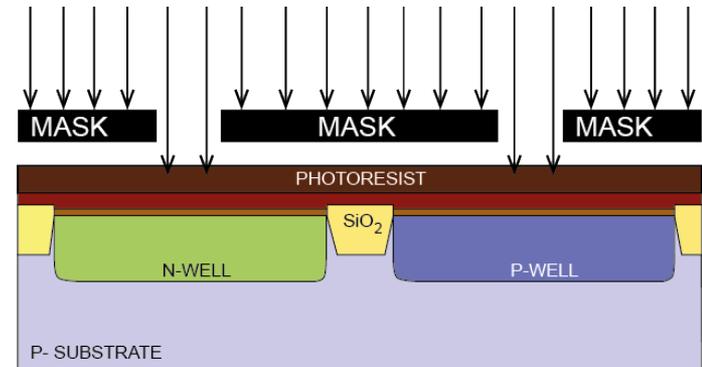
9. Gate oxide deposition



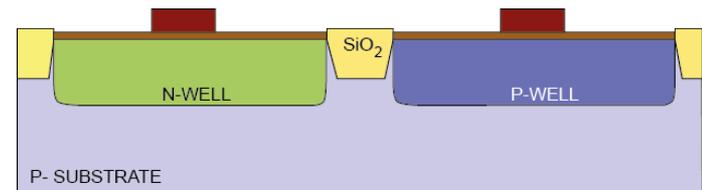
10. Deposition of polysilicon



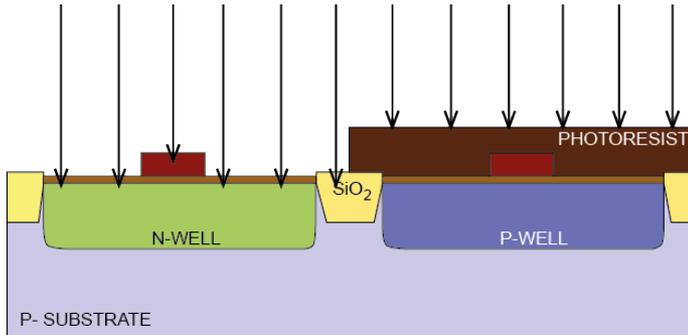
11. Photoresist deposition, illumination through mask



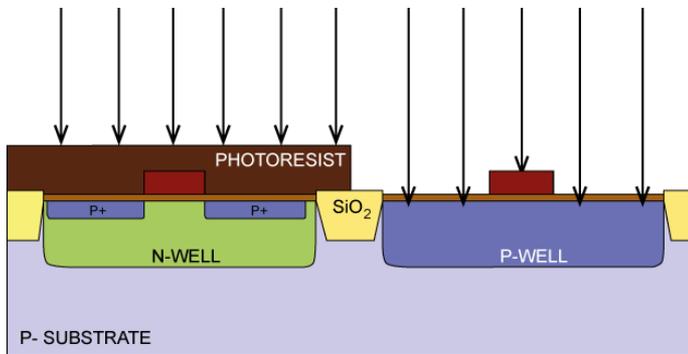
12. Gates are formed



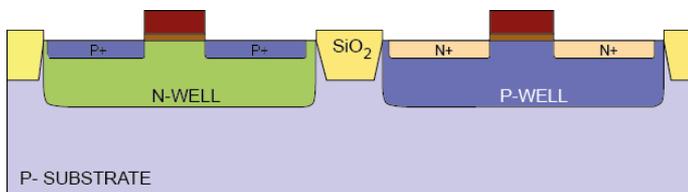
13. Low energy implantation of Boron dopants -> forming P+ regions of drain and source



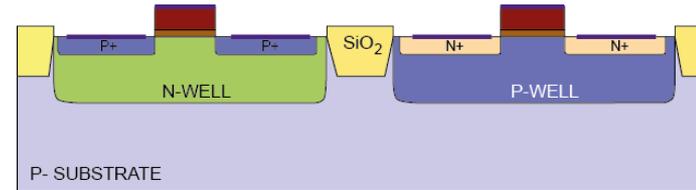
14. Low energy implantation of Phosphor dopants -> forming N+ regions of drain and source



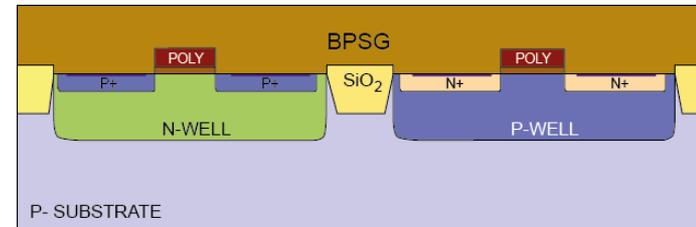
15. Removing photoresist and oxide from source and drain



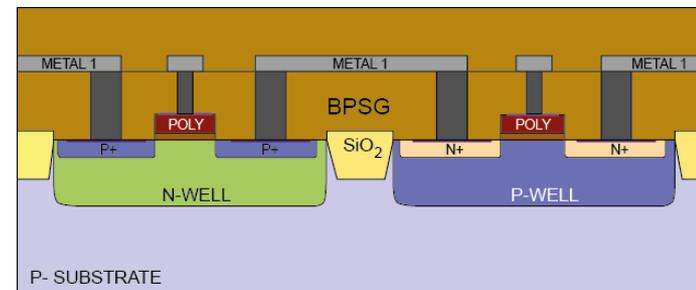
16. Silicidation



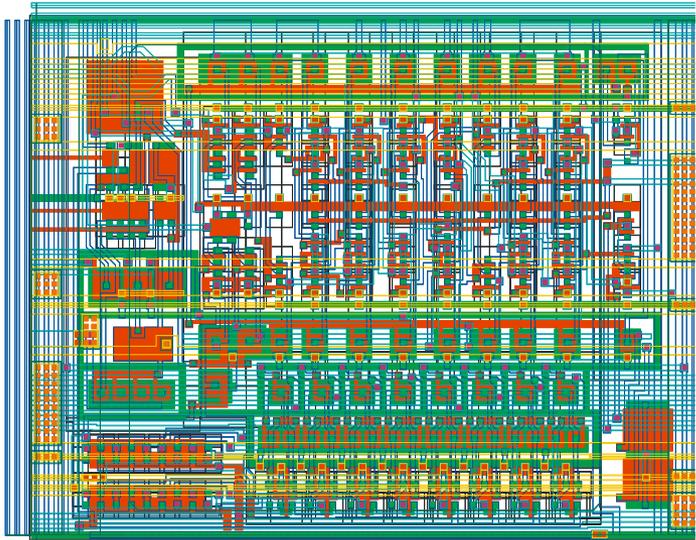
16. BPSG deposition



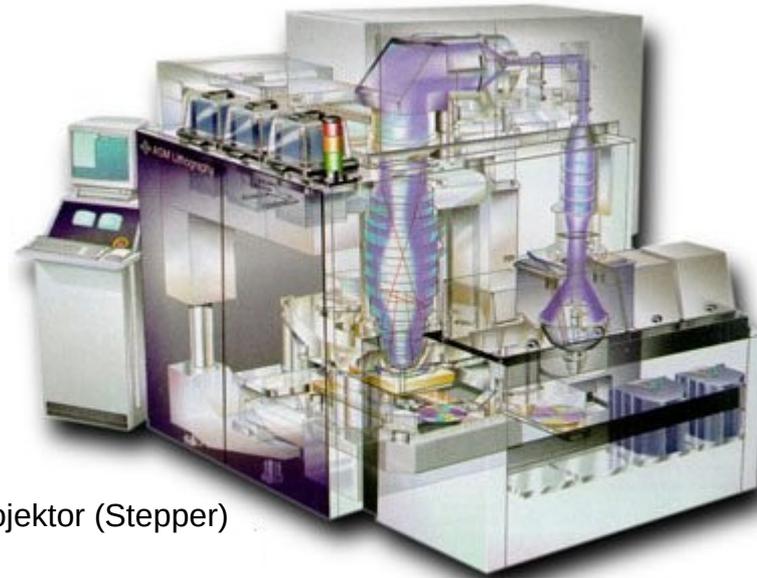
17. Etching, vias, deposition of METAL1, BPSG isolation



- Layout -> Fotomaske -> IC

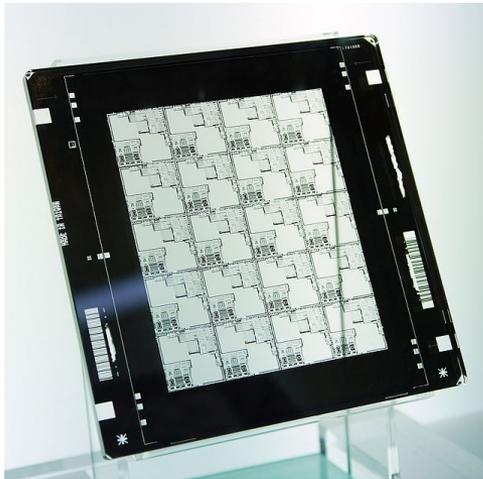


Layout

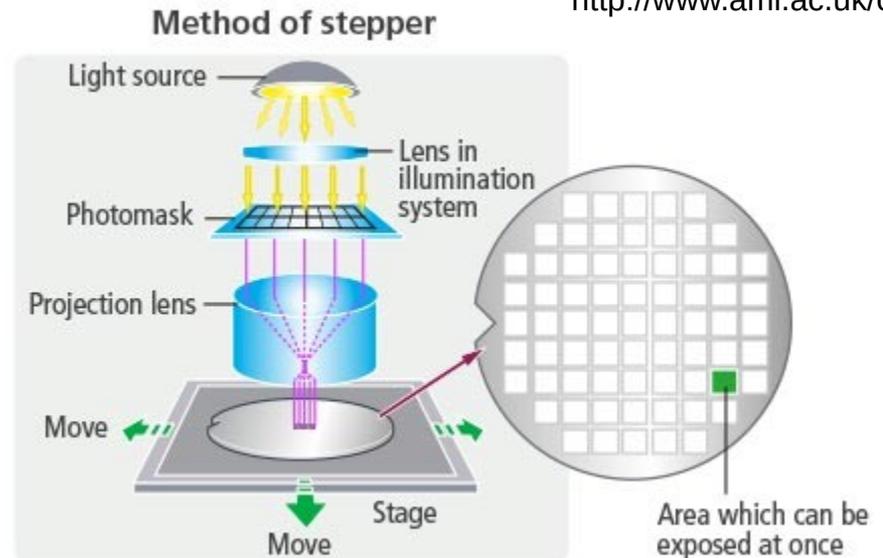


Projektor (Stepper)

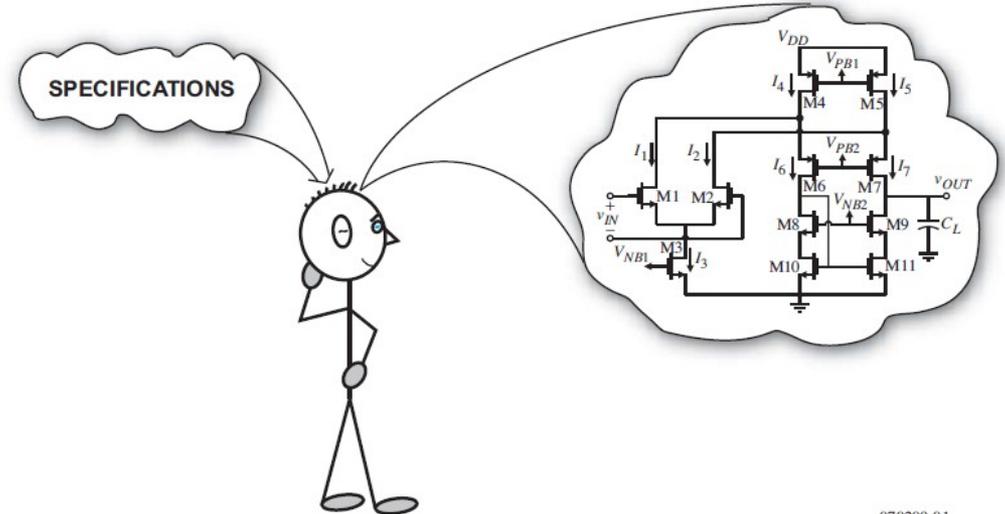
<http://www.ami.ac.uk/courses/>



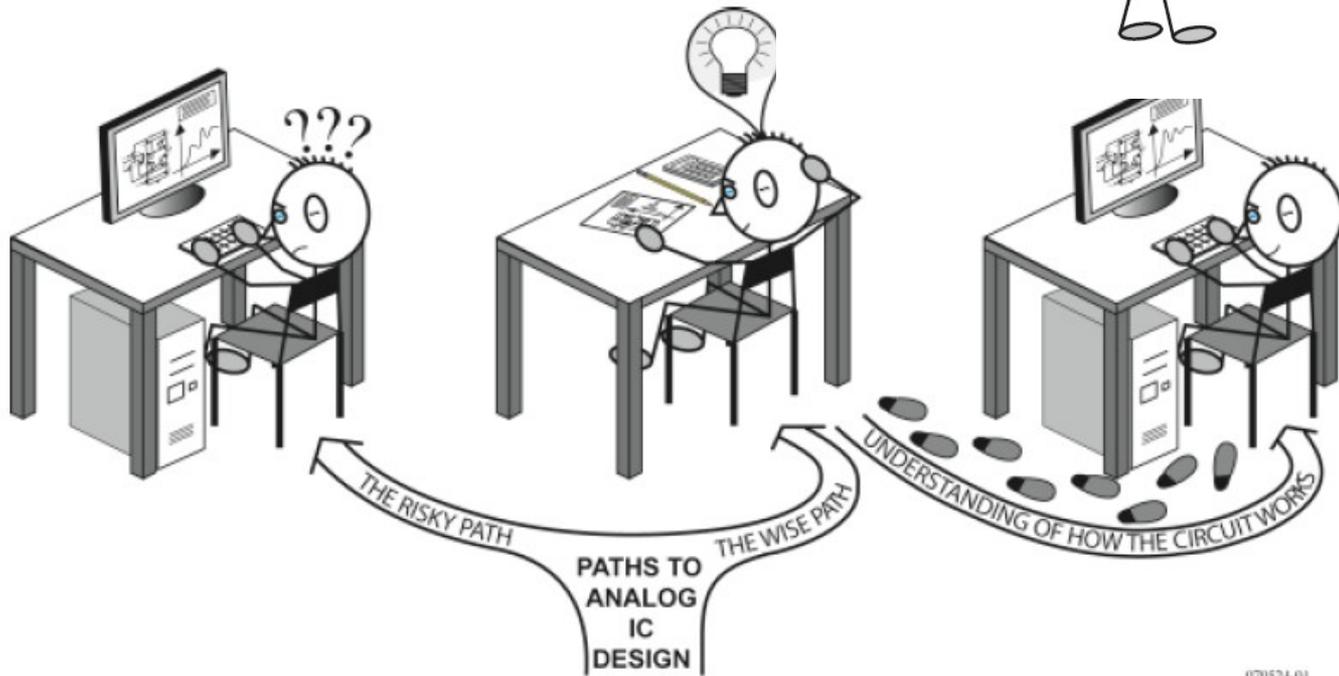
Maske



- IC Design Software (z.B. Cadence)
- Analog- und Digital-Design-Flow
- Spezifikationen
- Systemkonzept
- Schaltungstechnische Realisierung
- Wichtig (P.E. Allen):
- zuerst Schaltung verstehen
- und danach sich vorm PC setzten



070209-01

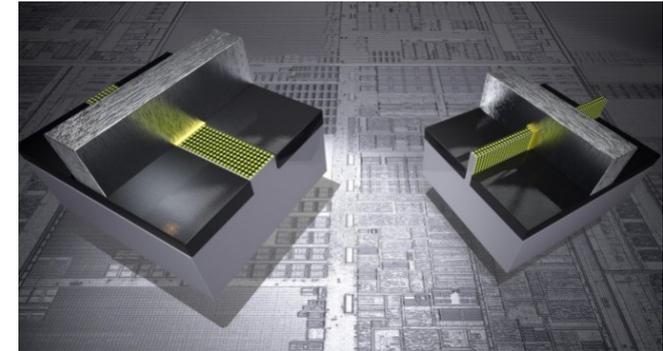


070524-01

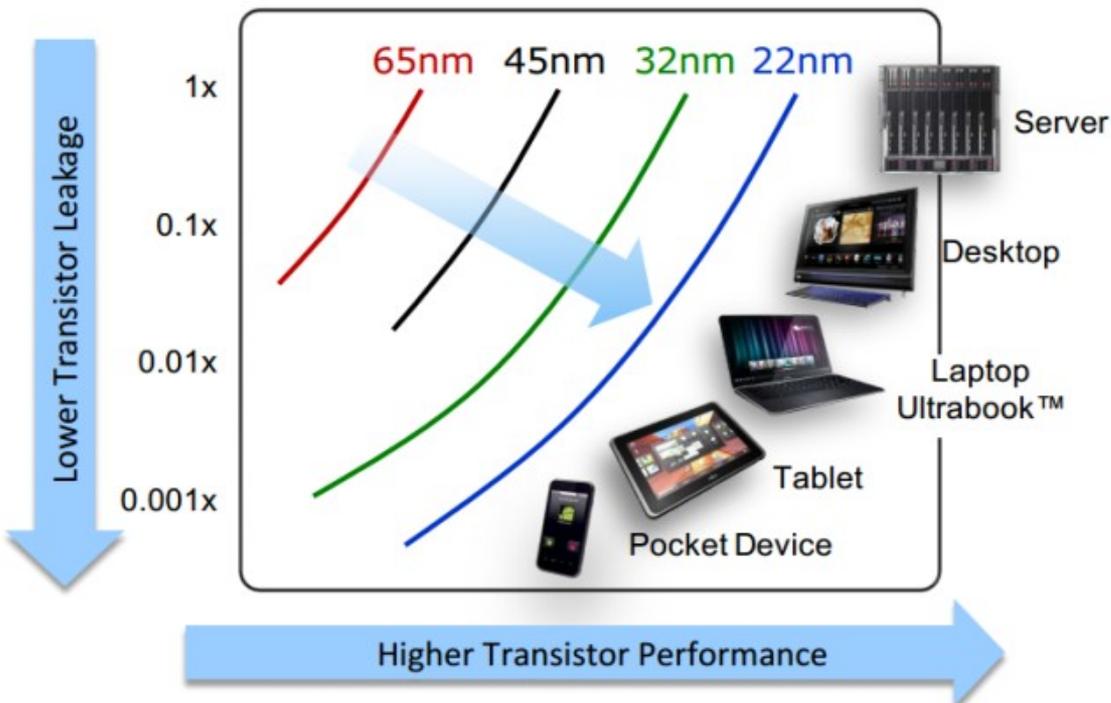
- Chiphersteller wählen („foundry“)



- Prozess wählen
- CMOS (digital, opto, analog, RF)
- Prozesse:
- SOI, BiCMOS, HVCMOS, FINFET, FD SOI
- Process nodes:
- 0.35 μm , 0.18 μm , 0.13 μm , 90nm, 65nm, 40nm, 28nm...
- Kleinere Prozesse – analog Design schwieriger
- Europractice: Multi Project Runs

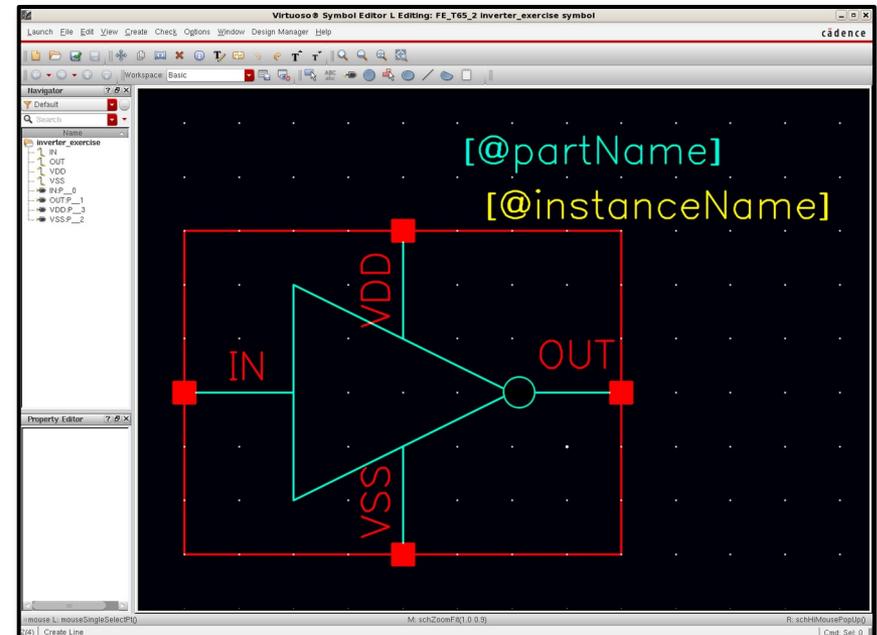
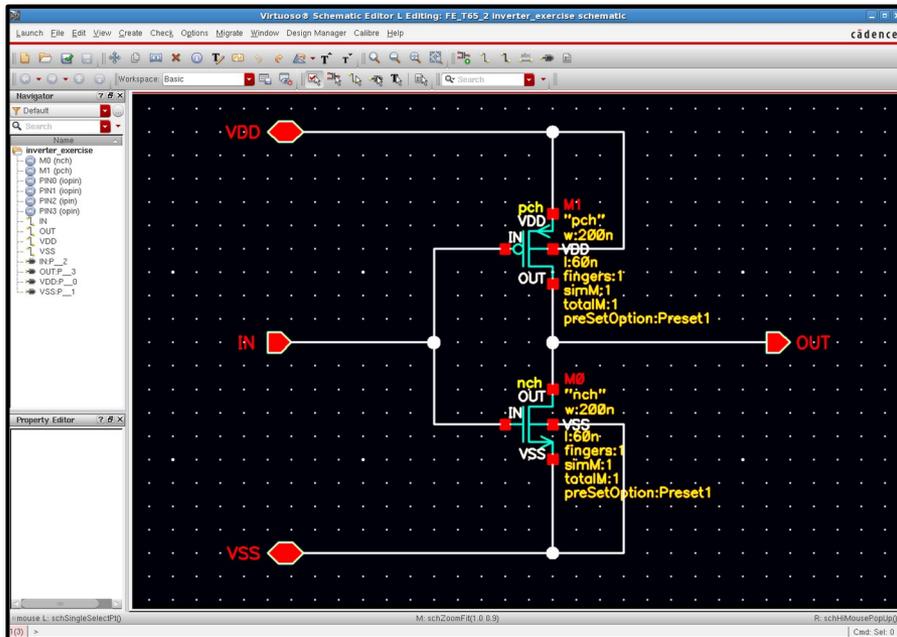


<http://www.extremetech.com/>

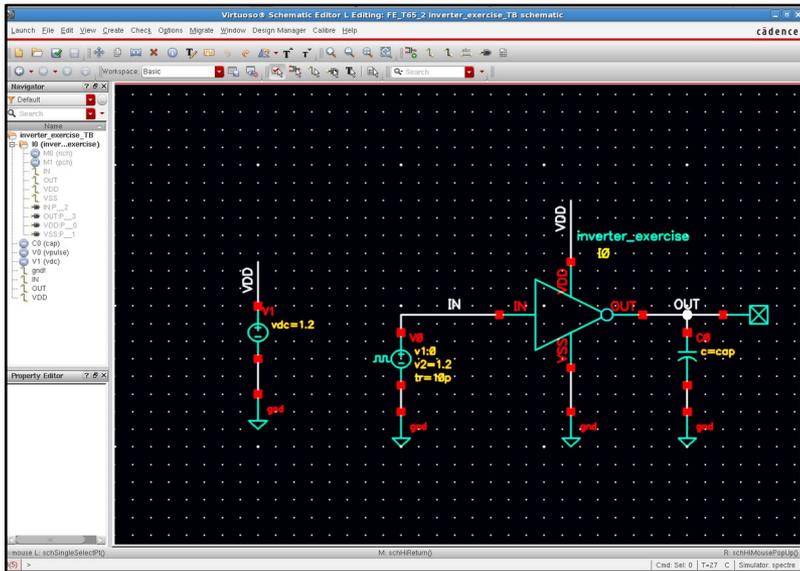


- Simulationsmodelle
- Layout-Regeln
- Process Design Kit (PDK) – Prozess-Bibliothek
- <http://www.europractice-ic.com/>

- Schaltplanentwurf im Schematics Editor
- Transistor, Hierarchie, Inputs/Outputs
- Symbol wird generiert – hierarchische Designs



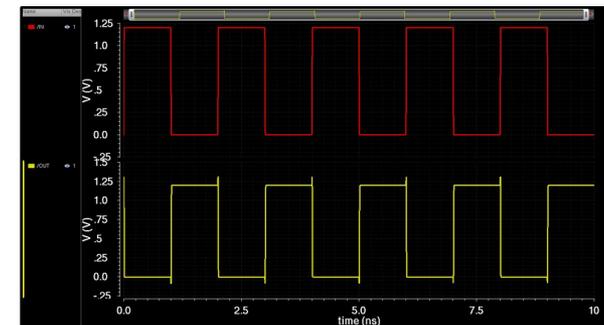
- Schaltung wird simuliert
- Analoge, mixed-mode- oder digitale Simulation
- AC, DC, Großsignale (Transient Analysis)



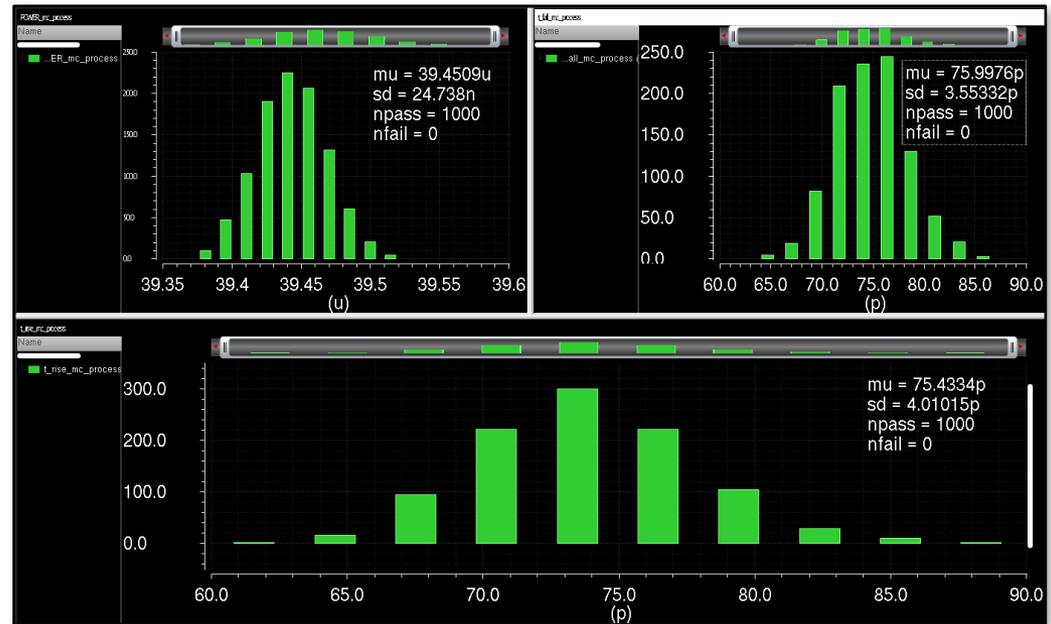
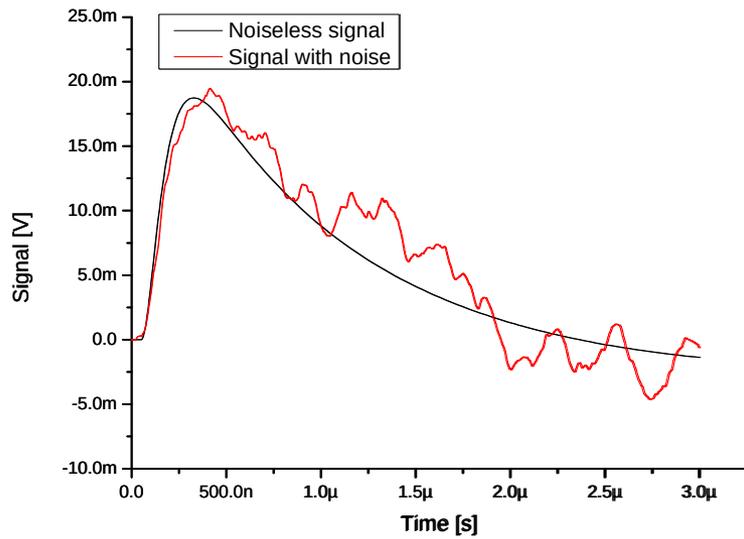
Test	Output	Normal	Spec	Weight	Pass/Fail
FE_T65_2_inverter_exercise_TB1 / IN	LC				
FE_T65_2_inverter_exercise_TB1 / OUT	LC				
FE_T65_2_inverter_exercise_TB1 / L_in	LC			4.188p	
FE_T65_2_inverter_exercise_TB1 / L_out	LC			8.535p	
FE_T65_2_inverter_exercise_TB1 / POWER	POWER			172.8h	
FE_T65_2_inverter_exercise_TB1 / AVDD					

Design Variables	Name	Value
with_2f		
with_p		
c1p		

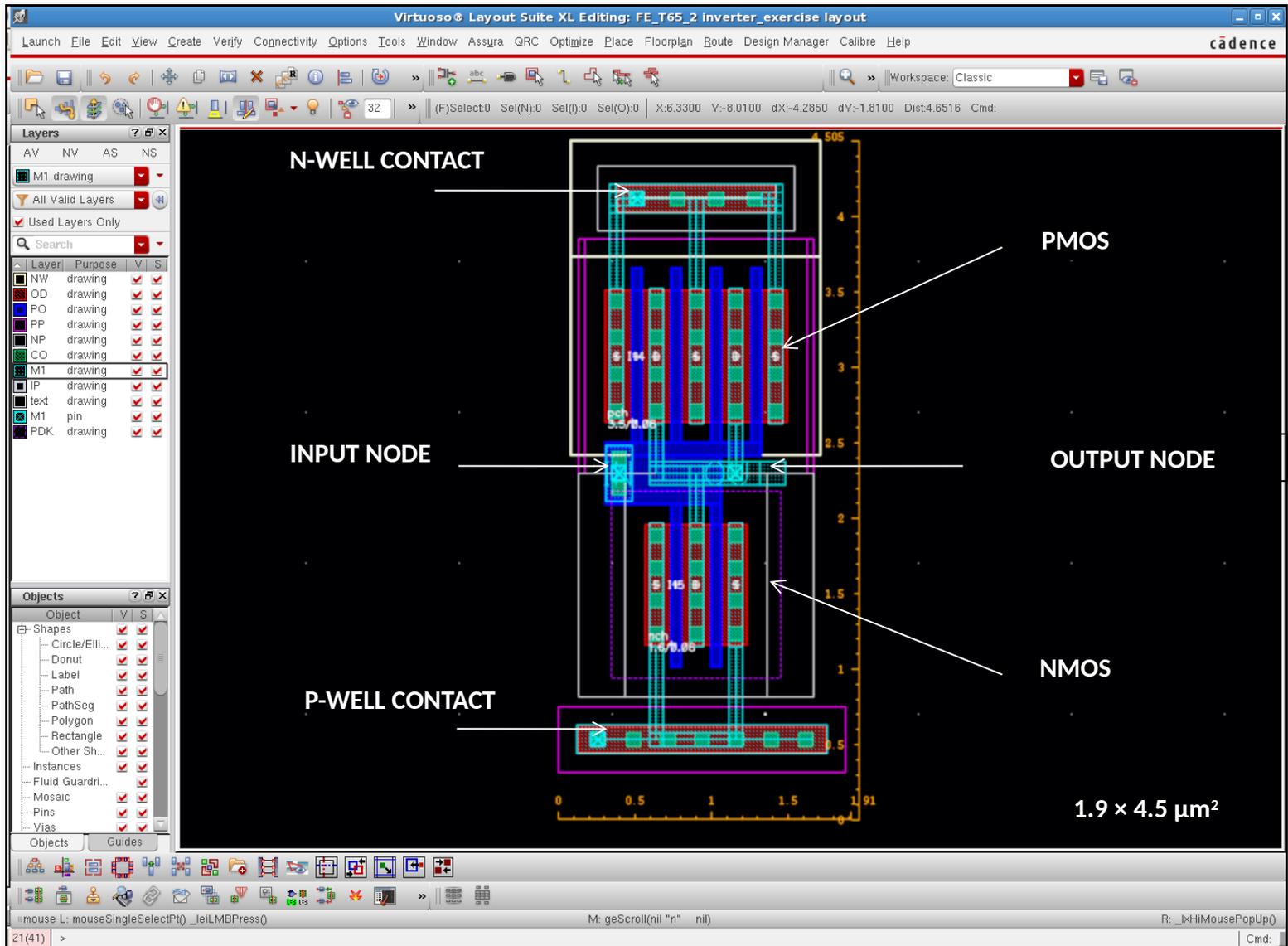
Outputs	Name/SignalExpr	Value	Plot	Save	Save Options
IN			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	altv
OUT			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	altv
L_in			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
L_out			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
POWER			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
AVDD			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	altv



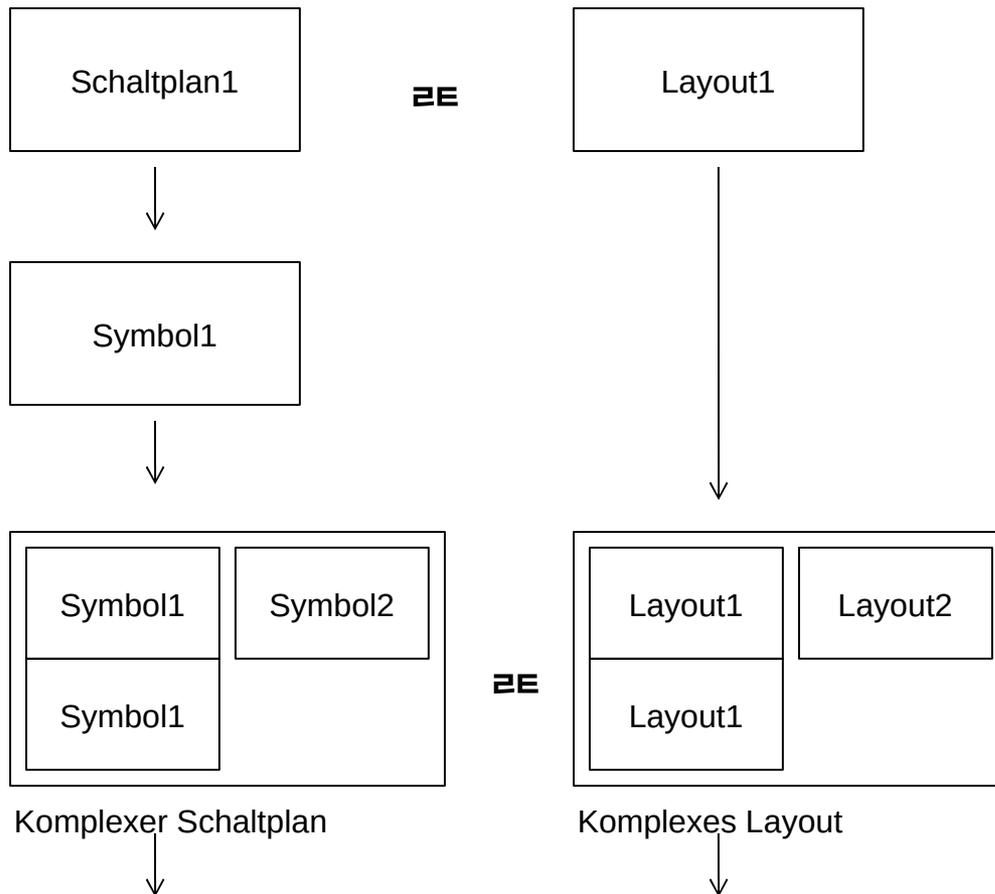
- Rauschen
- Mismatch



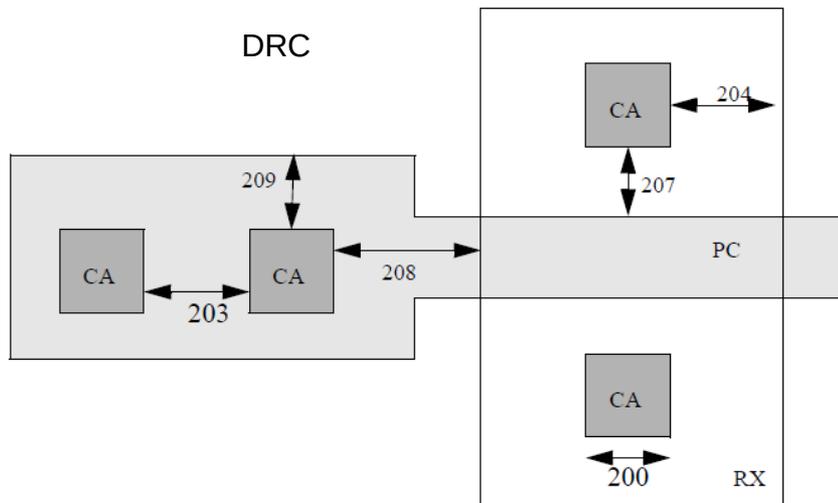
- Layout-Design
- Masken
- Transistoren „von oben“
- Analog Design – Full-Custom Layout (Hand-Layouted)



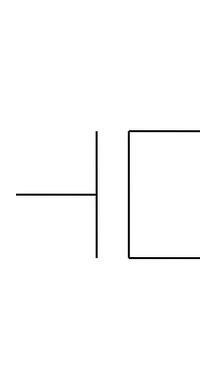
- Layout-Editor
- Polygone, Pfade
- Zellen, Blöcke, Hierarchie
- Semiautomatische Generierung von Layouts aus dem Schaltplan ist möglich



- Layout-Regeln (Teil vom PDK)
- DRC Überprüfung von Layout-Regeln
- LVS Layout Schaltplan Vergleich
- Layout -> Netzliste <-> Netzliste <- Schaltplan
- Extraktion von Kapazitäten aus Layout
- Post-Layout Simulation
- Evt. Anpassung vom Schaltplan notwendig



LVS

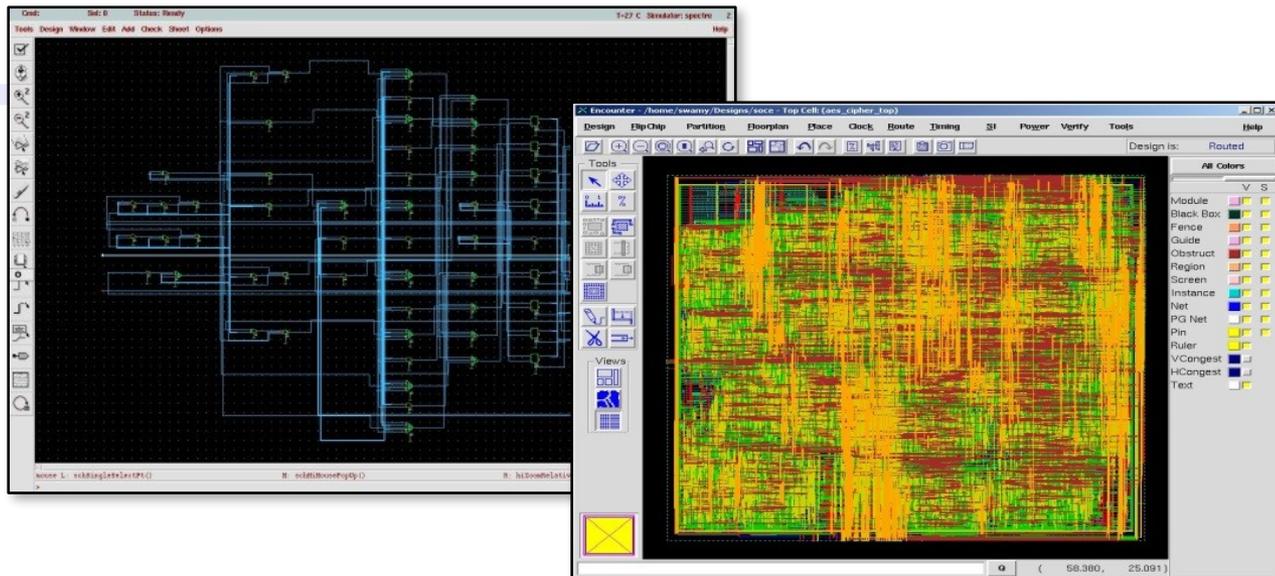


- Digitaldesign
- HDL Code, Simulation -> RTL Code (Schaltplan mit Logikzellen und Registern), Simulation (automatisch) -> Layout, Simulation (automatisch) -> DRC, LVS

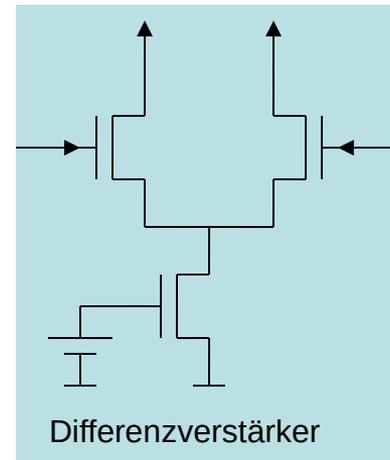
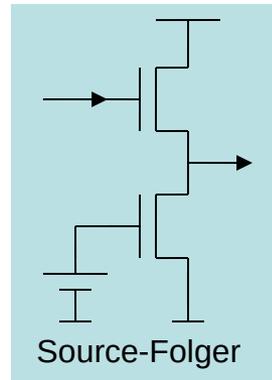
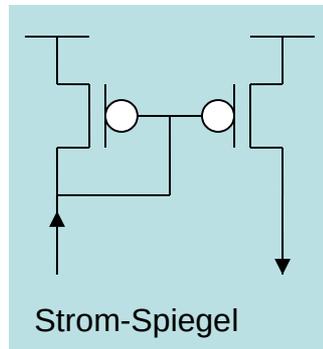
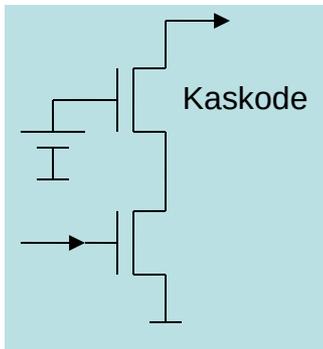
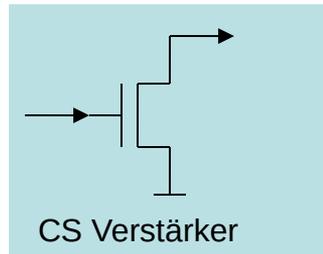
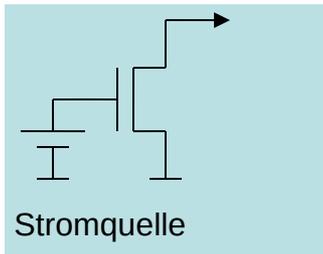
```

19 localparam IDCODE          = 4'b0010;
20 localparam INIT_IR_VALUE   = 4'b0101;
21
22
23 reg [IR_LENGTH-1:0] jtag_ir;           // Instruction register.
24
25 always @ (posedge tck or posedge trst)
26 begin
27     if (trst) begin
28         jtag_ir[IR_LENGTH-1:0] <= {IR_LENGTH{1'b0}}; // Why not set to IDCODE ??? TODO
29         latched_jtag_ir      <= IDCODE; // IDCODE selected after reset
30     end else if (state_capture_ir)
31         jtag_ir <= INIT_IR_VALUE;           // This value is fixed for easier fault detection ???
32     else if (state_shift_ir)
33         jtag_ir[IR_LENGTH-1:0] <= {tdi, jtag_ir[IR_LENGTH-1:1]};
34     else if (state_update_ir)
35         latched_jtag_ir <= jtag_ir;
36     end
37
38 always @ (negedge tck)
39 begin
40     serout <= jtag_ir[0];
41 end

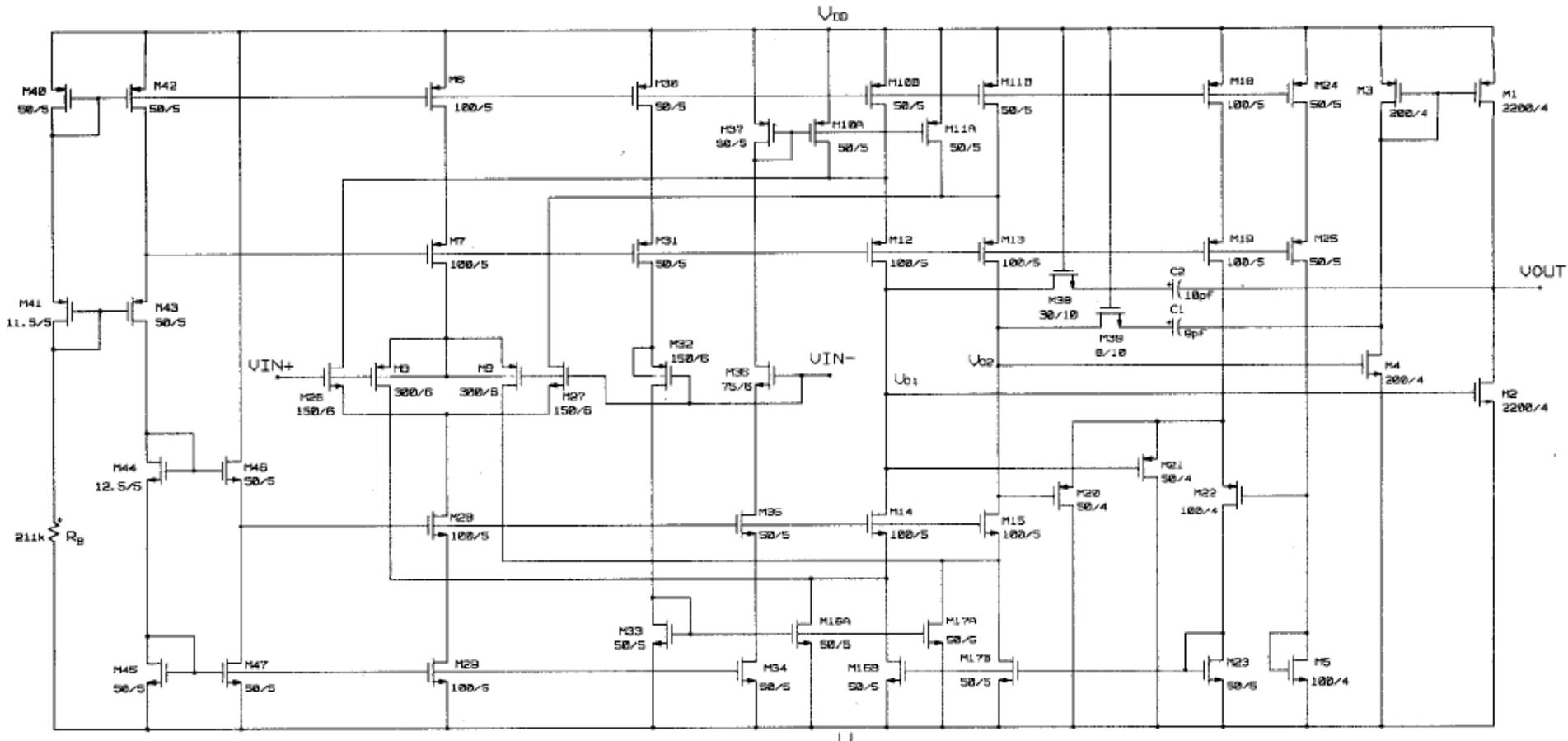
```



- Schaltungsentwurf
- Tricks:
- Gute Strukturierung
- Verwendung von Grundsaltungen
- Bausteinprinzip



- Verwendung von Grundschaltungen



Rail to rail CMOS Opamp: IEEE Journal of Solid-State Circuits, vol. 23, pp. 1414 – 1417, December 1988

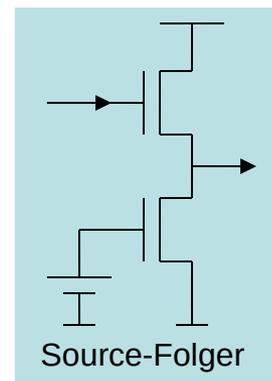
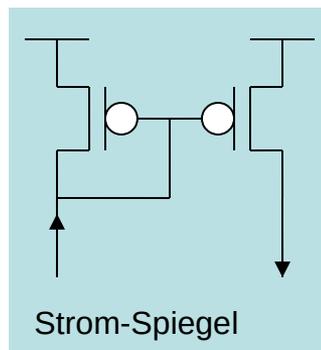
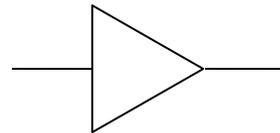
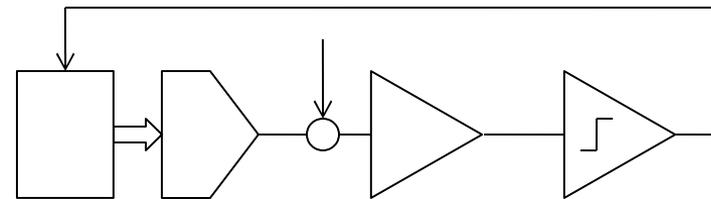
- Hierarchie im Chip

Chip (Integrierte Schaltung)

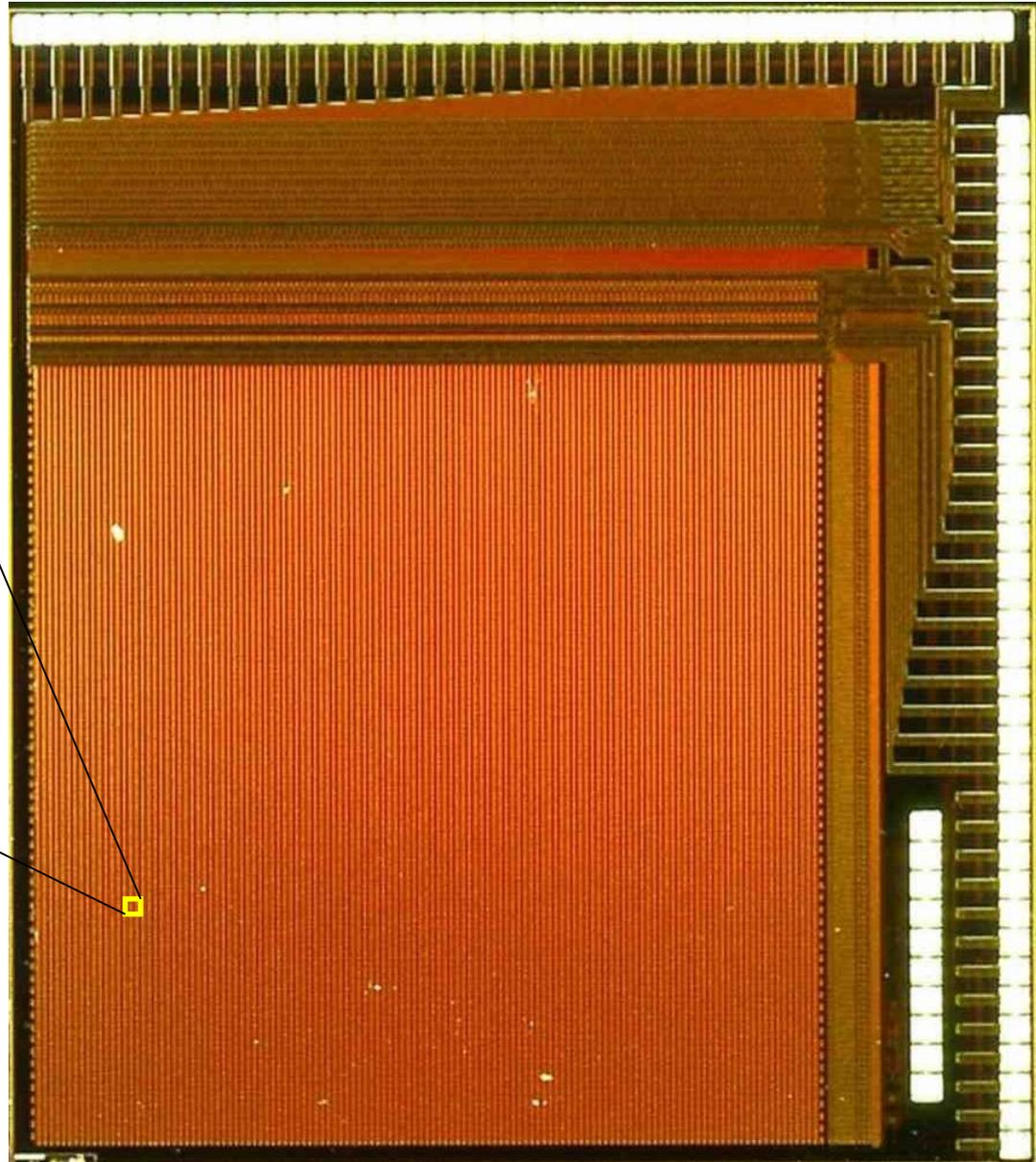
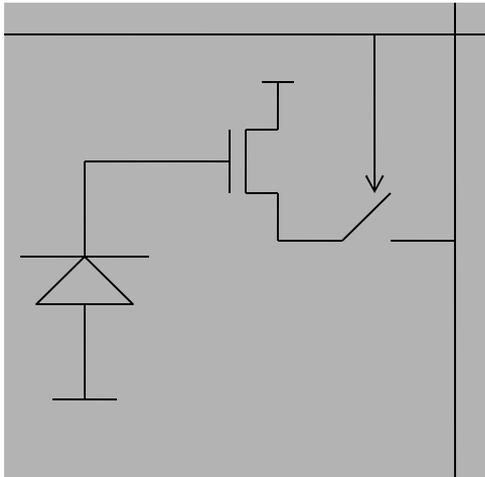
Systeme

Schaltungen

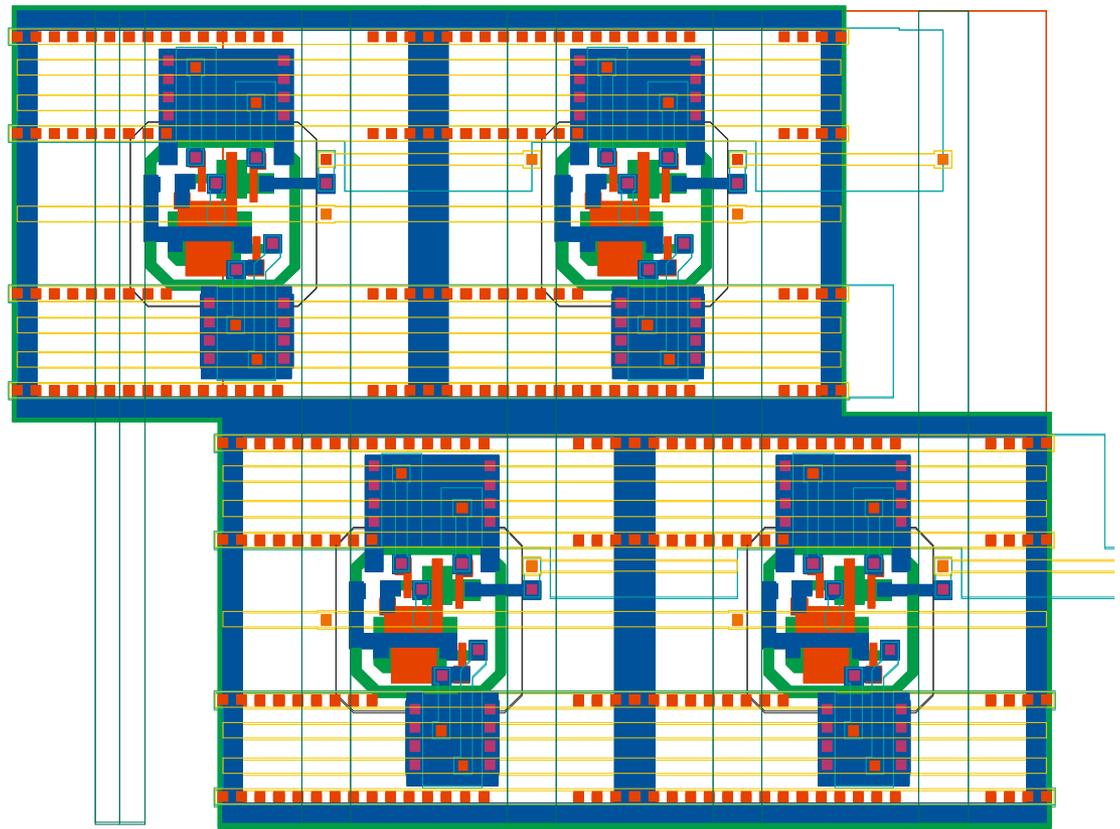
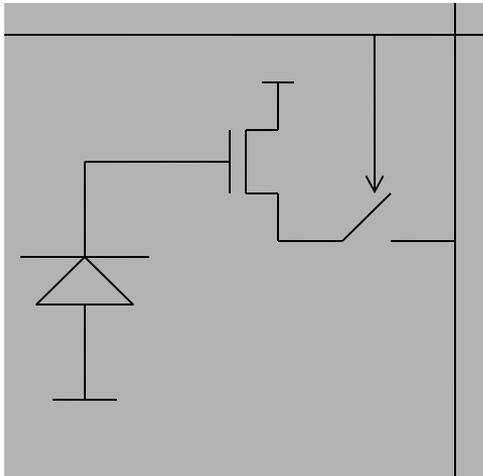
Grundsaltungen



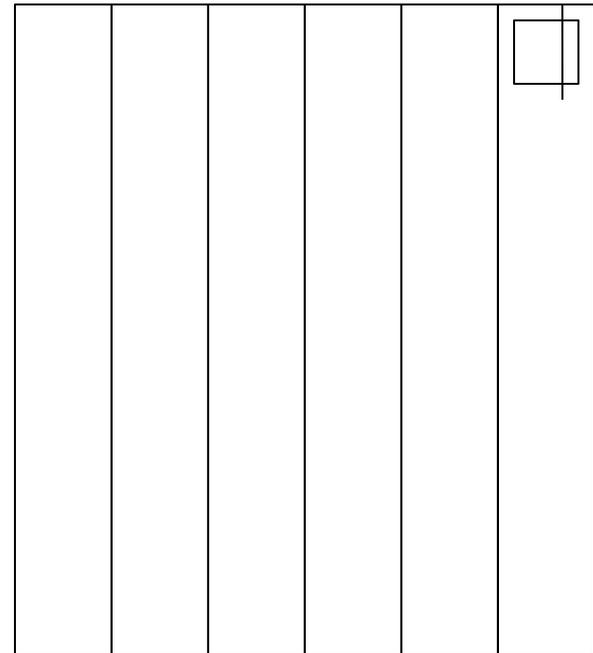
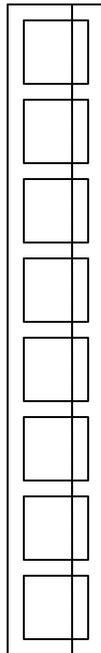
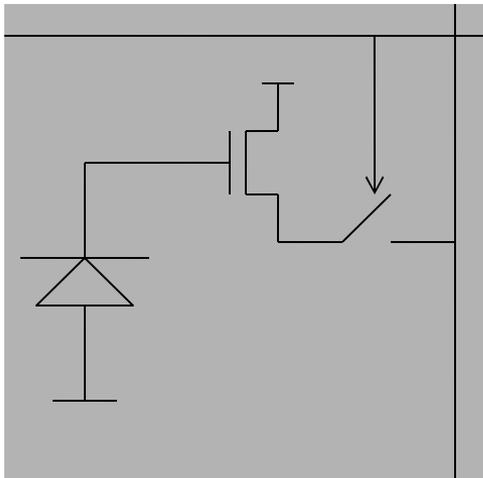
- Pixelsensor
- Pixel:
- Diode, Sensor
- Sourcefolger, Verstärker

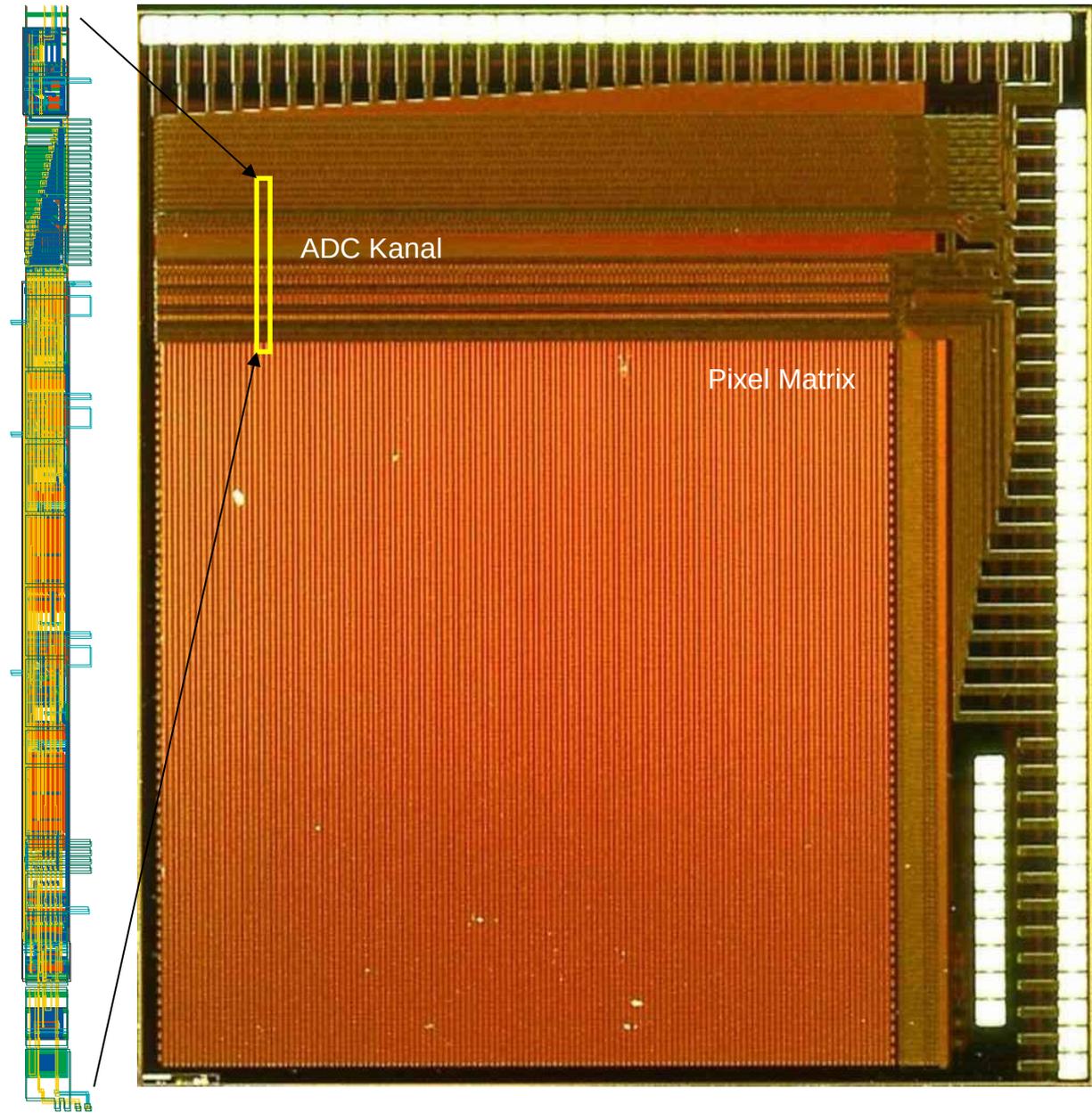


- Pixel Schaltplan
- Pixel Layout
- DRC, LVS

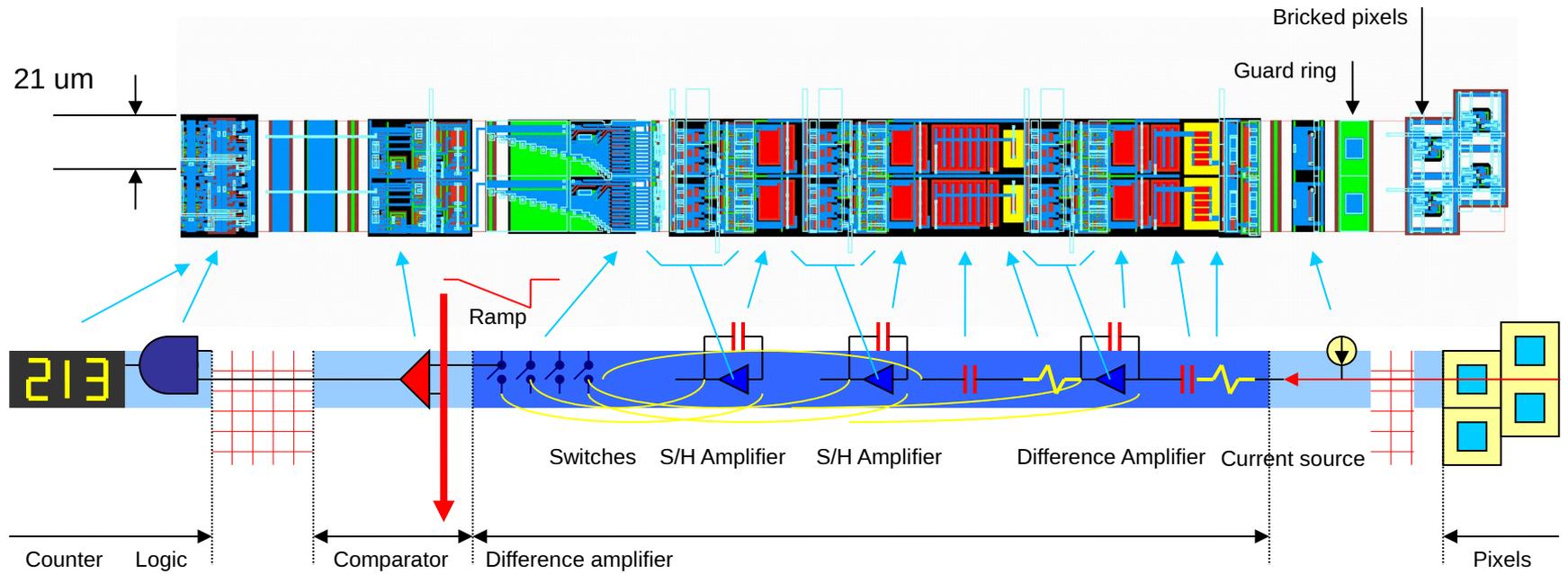


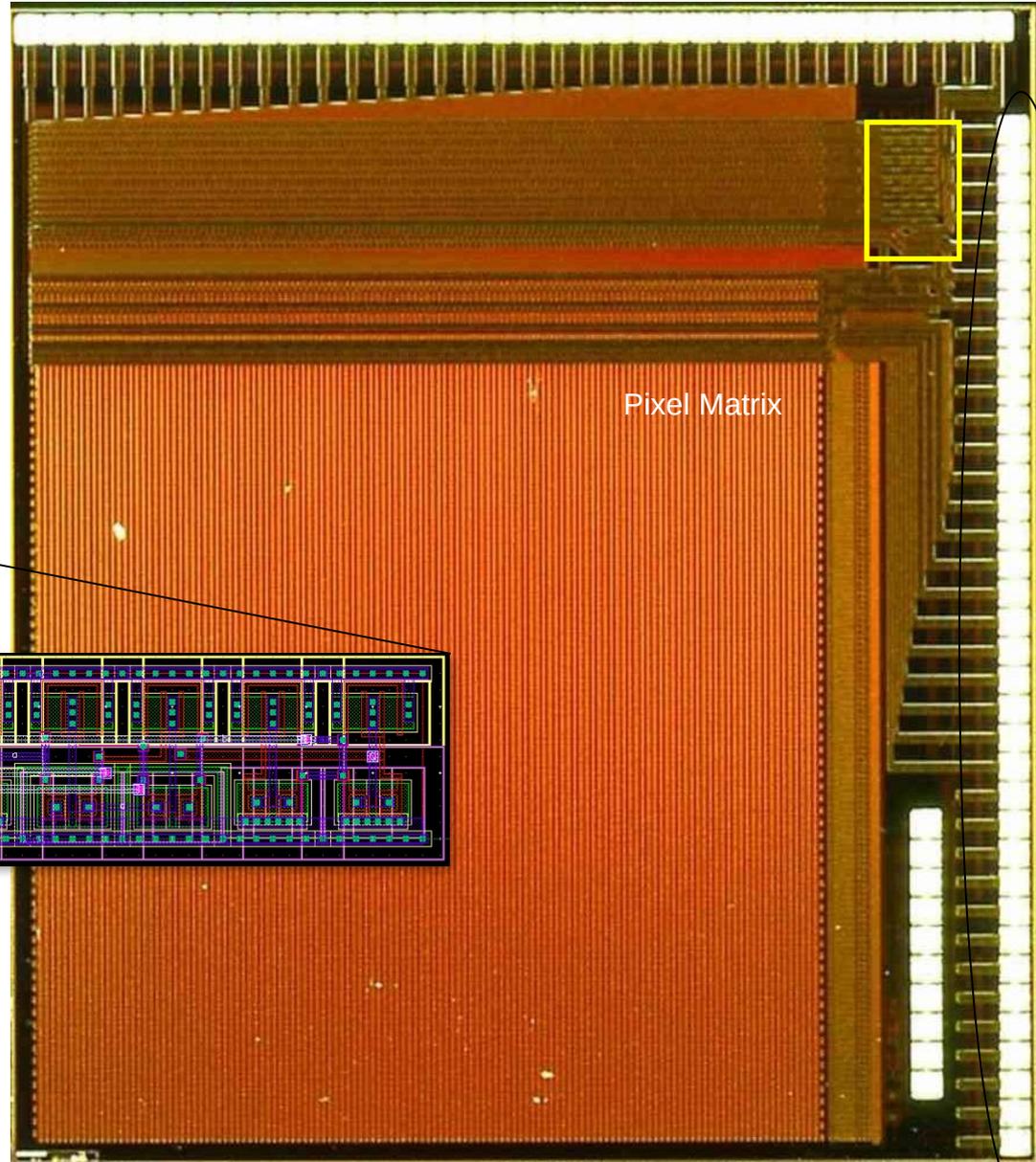
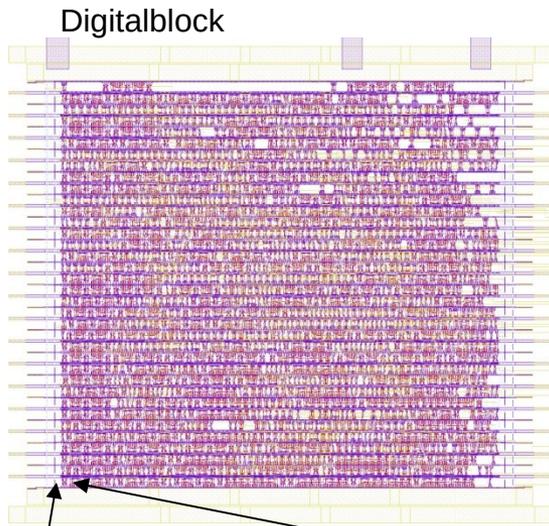
- Pixel
- Pixel Spalte
- Pixel Matrix





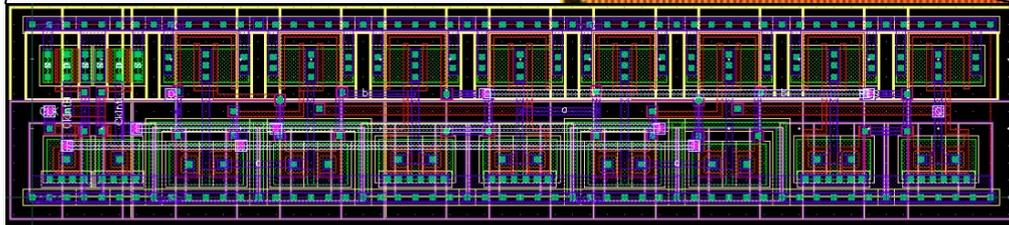
- ADC





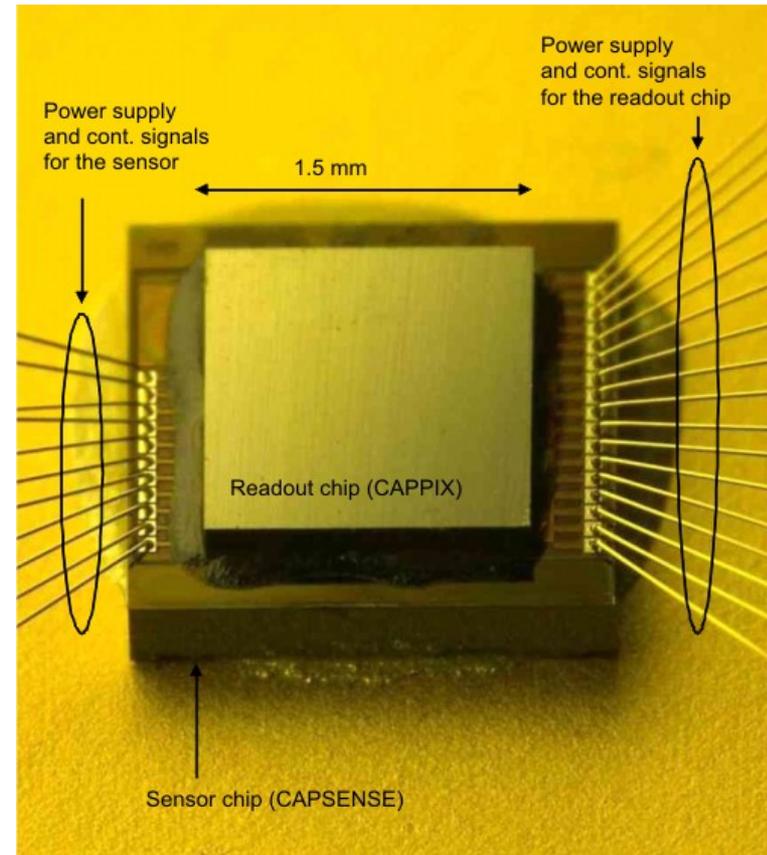
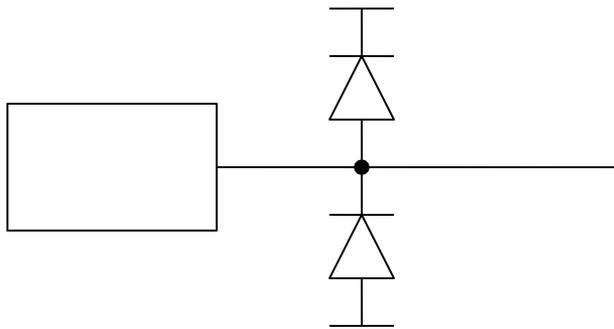
Pixel Matrix

IO Pads



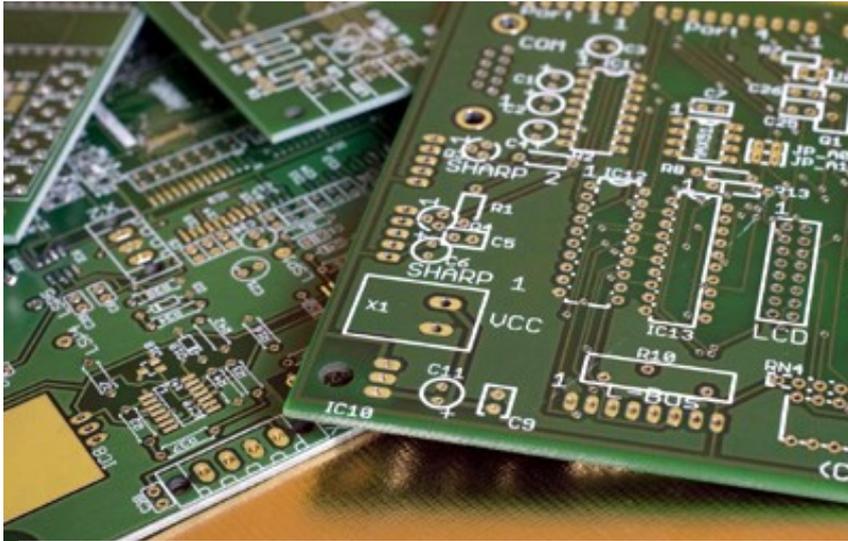
Logik-Zelle (Standardzelle)

- IO Pads
- Drahtbonden
- ESD protection (ESD Schutz)



- Design analoger Schaltungen
- Techniken:
- Gegenkopplung
- AC, DC Analyse
- Stabilitätskriterien

- Leiterplatten-Design
- Viele kommerziellen Komponenten



1.619 Produktergebnisse Für "Operationsverstärker"

<http://www.pcb-pool.com/>

<http://de.farnell.com/>

Produkte (1.619) | Datenblätter (0) | Community

Angewendete Filter

Anzahl der Verstärker: 1

Filter

- Produkt vorrätig
- RoHS-konform
- Neu
- In Kürze erhältlich
- Produkte ausschließen, die nicht für neue Designs empfohlen wurden
- Produkte aus erweitertem Sortiment ausschließen

Suche innerhalb von:

Filter auswählen: Filter automatisch aktualisieren

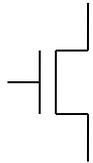
Versorgungsspannung	Bauform	Anzahl der Pins	Bandbreite	Betriebstemperatur, min.	Betriebstemperatur, max.	Verpackung
<input type="checkbox"/> - (1) <input type="checkbox"/> 0V bis 5V (1) <input type="checkbox"/> 1.1V bis 45V (2) <input type="checkbox"/> 1.1V bis 7V (1) <input type="checkbox"/> 1.4V bis 16V (2)	<input type="checkbox"/> BGA (1) <input type="checkbox"/> CFP (1) <input type="checkbox"/> CSP (1) <input type="checkbox"/> DFN (13) <input type="checkbox"/> DIP (205)	<input type="checkbox"/> 4 (4) <input type="checkbox"/> 5 (676) <input type="checkbox"/> 6 (108) <input type="checkbox"/> 7 (23) <input type="checkbox"/> 8 (767)	<input type="checkbox"/> - (4) <input type="checkbox"/> 1kHz (1) <input type="checkbox"/> 2kHz (2) <input type="checkbox"/> 2.5kHz (1) <input type="checkbox"/> 2.7kHz (3)	<input type="checkbox"/> -65°C (4) <input type="checkbox"/> -55°C (83) <input type="checkbox"/> -45°C (3) <input type="checkbox"/> -40°C (1269) <input type="checkbox"/> -25°C (21)	<input type="checkbox"/> 58°C (1) <input type="checkbox"/> 60°C (1) <input type="checkbox"/> 70°C (233) <input type="checkbox"/> 80°C (1) <input type="checkbox"/> 85°C (628)	<input type="checkbox"/> G <input type="checkbox"/> G <input type="checkbox"/> P <input type="checkbox"/> R <input type="checkbox"/> S
<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>	<input type="button" value="Min. auswählen"/> <input type="button" value="Max. auswählen"/>

Es wurden 1.619 Produkte zu Ihrer Auswahl gefunden

Anzeige von 1 - 25 von 1.619
 1 2 3 4 5 Weiter

- IC-Design
- Nur zwei Grundkomponenten
- MOSFET als Verstärker, Stromquelle, Widerstand, Kondensator, Schalter, Diode verwendet
- Komplizierte MOSFET Modelle

- Komplizierte MOSFET Modelle



```

48 * SUBCIRCUIT SCHEMATIC:
49 *
50 *
51 *
52 *
53 *
54 *
55 *
56 *
57 *
58 *
59 *
60 *
61 *
62 *
63 *
64 *
65 *
66 *
67 *
68 *
69 *
70 *
71 *
72 *
73 *
74 *
75 *
76 *
77 *
78 *
79 *
80 *
81 *
82 *
83 *
84 *
85 *
86 *
87 *
88 *
89 *
90 *
91 *
92 *
93 *
94 *
95 *
96 *
97 *
98 *
99 *
100 *
101 *
102 *
103 *
104 *
105 *
106 *
107 *
108 *
109 *
110 *
111 *
112 *
113 *
114 *
115 *
116 *
117 *
118 *
119 *
120 *
121 *
122 *
123 *
124 *
125 *
126 *
127 *
128 *
129 *
130 *
131 *
132 *
133 *
134 *
135 *
136 *
137 *
138 *
139 *
140 *
141 *
142 *
143 *
144 *
145 *
146 *
147 *
148 *
149 *
150 *
151 *
152 *
153 *
154 *
155 *
156 *
157 *
158 *
159 *
160 *
161 *
162 *
163 *
164 *
165 *
166 *
167 *
168 *
169 *
170 *
171 *
172 *
173 *
174 *
175 *
176 *
177 *
178 *
179 *
180 *
181 *
182 *
183 *
184 *
185 *
186 *
187 *
188 *
189 *
190 *
191 *
192 *
193 *
194 *
195 *
196 *
197 *
198 *
199 *
200 *
201 *
202 *
203 *
204 *
205 *
206 *
207 *
208 *
209 *
210 *
211 *
212 *
213 *
214 *
215 *
216 *
217 *
218 *
219 *
220 *
221 *
222 *
223 *
224 *
225 *
226 *
227 *
228 *
229 *
230 *
231 *
232 *
233 *
234 *
235 *
236 *
237 *
238 *
239 *
240 *
241 *
242 *
243 *
244 *
245 *
246 *
247 *
248 *
249 *
250 *
251 *
252 *
253 *
254 *
255 *
256 *
257 *
258 *
259 *
260 *
261 *
262 *
263 *
264 *
265 *
266 *
267 *
268 *
269 *
270 *
271 *
272 *
273 *
274 *
275 *
276 *
277 *
278 *
279 *
280 *
281 *
282 *
283 *
284 *
285 *
286 *
287 *
288 *
289 *
290 *
291 *
292 *
293 *
294 *
295 *
296 *
297 *
298 *
299 *
300 *
301 *
302 *
303 *
304 *
305 *
306 *
307 *
308 *
309 *
310 *
311 *
312 *
313 *
314 *
315 *
316 *
317 *
318 *
319 *
320 *
321 *
322 *
323 *
324 *
325 *
326 *
327 *
328 *
329 *
330 *
331 *
332 *
333 *
334 *
335 *
336 *
337 *
338 *
339 *
340 *
341 *
342 *
343 *
344 *
345 *
346 *
347 *
348 *
349 *
350 *
351 *
352 *
353 *
354 *
355 *
356 *
357 *
358 *
359 *
360 *
361 *
362 *
363 *
364 *
365 *
366 *
367 *
368 *
369 *
370 *
371 *
372 *
373 *
374 *
375 *
376 *
377 *
378 *
379 *
380 *
381 *
382 *
383 *
384 *
385 *
386 *
387 *
388 *
389 *
390 *
391 *
392 *
393 *
394 *
395 *
396 *
397 *
398 *
399 *
400 *
401 *
402 *
403 *
404 *
405 *
406 *
407 *
408 *
409 *
410 *
411 *
412 *
413 *
414 *
415 *
416 *
417 *
418 *
419 *
420 *
421 *
422 *
423 *
424 *
425 *
426 *
427 *
428 *
429 *
430 *
431 *
432 *
433 *
434 *
435 *
436 *
437 *
438 *
439 *
440 *
441 *
442 *
443 *
444 *
445 *
446 *
447 *
448 *
449 *
450 *
451 *
452 *
453 *
454 *
455 *
456 *
457 *
458 *
459 *
460 *
461 *
462 *
463 *
464 *
465 *
466 *
467 *
468 *
469 *
470 *
471 *
472 *
473 *
474 *
475 *
476 *
477 *
478 *
479 *
480 *
481 *
482 *
483 *
484 *
485 *
486 *
487 *
488 *
489 *
490 *
491 *
492 *
493 *
494 *
495 *
496 *
497 *
498 *
499 *
500 *
501 *
502 *
503 *
504 *
505 *
506 *
507 *
508 *
509 *
510 *
511 *
512 *
513 *
514 *
515 *
516 *
517 *
518 *
519 *
520 *
521 *
522 *
523 *
524 *
525 *
526 *
527 *
528 *
529 *
530 *
531 *
532 *
533 *
534 *
535 *
536 *
537 *
538 *
539 *
540 *
541 *
542 *
543 *
544 *
545 *
546 *
547 *
548 *
549 *
550 *
551 *
552 *
553 *
554 *
555 *
556 *
557 *
558 *
559 *
560 *
561 *
562 *
563 *
564 *
565 *
566 *
567 *
568 *
569 *
570 *
571 *
572 *
573 *
574 *
575 *
576 *
577 *
578 *
579 *
580 *
581 *
582 *
583 *
584 *
585 *
586 *
587 *
588 *
589 *
590 *
591 *
592 *
593 *
594 *
595 *
596 *
597 *
598 *
599 *
600 *
601 *
602 *
603 *
604 *
605 *
606 *
607 *
608 *
609 *
610 *
611 *
612 *
613 *
614 *
615 *
616 *
617 *
618 *
619 *
620 *
621 *
622 *
623 *
624 *
625 *
626 *
627 *
628 *
629 *
630 *
631 *
632 *
633 *
634 *
635 *
636 *
637 *
638 *
639 *
640 *
641 *
642 *
643 *
644 *
645 *
646 *
647 *
648 *
649 *
650 *
651 *
652 *
653 *
654 *
655 *
656 *
657 *
658 *
659 *
660 *
661 *
662 *
663 *
664 *
665 *
666 *
667 *
668 *
669 *
670 *
671 *
672 *
673 *
674 *
675 *
676 *
677 *
678 *
679 *
680 *
681 *
682 *
683 *
684 *
685 *
686 *
687 *
688 *
689 *
690 *
691 *
692 *
693 *
694 *
695 *
696 *
697 *
698 *
699 *
700 *
701 *
702 *
703 *
704 *
705 *
706 *
707 *
708 *
709 *
710 *
711 *
712 *
713 *
714 *
715 *
716 *
717 *
718 *
719 *
720 *
721 *
722 *
723 *
724 *
725 *
726 *
727 *
728 *
729 *
730 *
731 *
732 *
733 *
734 *
735 *
736 *
737 *
738 *
739 *
740 *
741 *
742 *
743 *
744 *
745 *
746 *
747 *
748 *
749 *
750 *
751 *
752 *
753 *
754 *
755 *
756 *
757 *
758 *
759 *
760 *
761 *
762 *
763 *
764 *
765 *
766 *
767 *
768 *
769 *
770 *
771 *
772 *
773 *
774 *
775 *
776 *
777 *
778 *
779 *
780 *
781 *
782 *
783 *
784 *
785 *
786 *
787 *
788 *
789 *
790 *
791 *
792 *
793 *
794 *
795 *
796 *
797 *
798 *
799 *
800 *
801 *
802 *
803 *
804 *
805 *
806 *
807 *
808 *
809 *
810 *
811 *
812 *
813 *
814 *
815 *
816 *
817 *
818 *
819 *
820 *
821 *
822 *
823 *
824 *
825 *
826 *
827 *
828 *
829 *
830 *
831 *
832 *
833 *
834 *
835 *
836 *
837 *
838 *
839 *
840 *
841 *
842 *
843 *
844 *
845 *
846 *
847 *
848 *
849 *
850 *
851 *
852 *
853 *
854 *
855 *
856 *
857 *
858 *
859 *
860 *
861 *
862 *
863 *
864 *
865 *
866 *
867 *
868 *
869 *
870 *
871 *
872 *
873 *
874 *
875 *
876 *
877 *
878 *
879 *
880 *
881 *
882 *
883 *
884 *
885 *
886 *
887 *
888 *
889 *
890 *
891 *
892 *
893 *
894 *
895 *
896 *
897 *
898 *
899 *
900 *
901 *
902 *
903 *
904 *
905 *
906 *
907 *
908 *
909 *
910 *
911 *
912 *
913 *
914 *
915 *
916 *
917 *
918 *
919 *
920 *
921 *
922 *
923 *
924 *
925 *
926 *
927 *
928 *
929 *
930 *
931 *
932 *
933 *
934 *
935 *
936 *
937 *
938 *
939 *
940 *
941 *
942 *
943 *
944 *
945 *
946 *
947 *
948 *
949 *
950 *
951 *
952 *
953 *
954 *
955 *
956 *
957 *
958 *
959 *
960 *
961 *
962 *
963 *
964 *
965 *
966 *
967 *
968 *
969 *
970 *
971 *
972 *
973 *
974 *
975 *
976 *
977 *
978 *
979 *
980 *
981 *
982 *
983 *
984 *
985 *
986 *
987 *
988 *
989 *
990 *
991 *
992 *
993 *
994 *
995 *
996 *
997 *
998 *
999 *
1000 *

```

B.1.6 Drain Current Expression

$$I_{ds} = \frac{I_{dso}(V_{dseff})}{1 + \frac{R_{ds} I_{dso}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCRBE}} \right)$$

$$I_{dso} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff} (1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2V_t)}) V_{dseff}}{L_{eff} [1 + V_{dseff} / (E_{sat} L_{eff})]}$$

$$V_A = V_{Asat} + (1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat} l_{itl}} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2V_t)}{\theta_{rout} (1 + P_{DIBLC} V_{dseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2V_t} \right)$$

```

177 * Core Parameters
178 *****
179 + a11 = -0.0284 + stthesatl = -0.0135
180 + a10 = 22.22285 + stthesatlw = 0.00564
181 + a1w = 0.1286 + stthesato = 1.231
182 + a20 = 18.9287 + stthesatw = -0.1331
183 + a31 = -0.08288 + stvfbl = 0.01
184 + a30 = 1.016289 + stvfblw = 0.001
185 + a3w = 0.01290 + stvfbo = 0.0008728
186 + a41 = 0.005291 + stvfbo = 0.0254
187 + a40 = 0.015292 + stxcoro = 2
188 + a4w = -1293 + themuo = 2.4
189 + agidlw = 0.0294 + thesatbo = 0.1
190 + alp111 = 0.0295 + thesatgo = 0.2126
191 + alp112 = 1.1296 + thesatlexp = 0.8524
192 + alp1lexp = 0297 + thesatlw = 0.00566
193 + alp1w = -0.0298 + thesato = 0.0108
194 + alp211 = 0.0299 + thesatw = -0.08
195 + alp212 = 0.1300 + tkuo = 0
196 + alp2lexp = 1301 + vfbw = -0.011
197 + alp2w = -5302 + vnsubo = 0
198 + alp1 = 0.018303 + vpo = 0.09954
199 + alp1exp = 0304 + wbet = 2.039E-08
200 + alp1w = -0.0305 + wkuo = 0
201 + ax1 = 0.4502306 + wkvtho = 0
202 + axo = 22.12307 + wlod = 0
203 + betw1 = 0.1308 + wlodkuo = 0
204 + betw2 = -0.0309 + wlodvth = 0
310 + wseg = 1E-08
311 + wseap = 5.444E-09

```

- Widerstand und Diode selten benutzt
- Kondensatoren ersetzt Widerstände
- MOSFETs ersetzen Dioden
- Transkonduktor

- Inhalt des Kurses:
- Approximative Methode für Schaltungsanalyse
- Analyse von Schaltungen mit Rückkopplung
- Berechnung von Zeitkonstanten
- Stabilitätskriterien
- Verstärkern
- Komplexere Schaltungen
- Mehrstufige-, differenzielle-, Rail to Rail-Verstärkern, Komparatoren
- Systeme: Switched Capacitor Schaltungen, ADCs
- Jede zweite Woche Übungen mit Chipdesign-Software
- Prüfung – Mündliche Prüfung – Beispiele aus den Übungen

- Literatur
- **Design of Analog CMOS Integrated Circuits** von Behzad Razavi
- **Operation and Modeling of the MOS Transistor**, Yannis Tsividis, Colin McAndrew
- **Analog Integrated Circuit Design**, David A. Jones, Ken Martin, John Wiley & Sons, Inc
- **Analysis and Design of Analog Integrated Circuits**, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, Inc
- **The Art of Analog Layout**, Alan Hastings, Prentice Hall
- **CMOS Analog Circuit Design**, Allen-Holberg, Oxford Press, 1987
- **Analog Design Essentials**, W. Sansen, Kluwer International Series in Engineering and Computer Science
- **Microelectronics** von Jacob Millman von T (1999)

- Themen
- 1 Rückkopplung, Formeln für Schaltungen mit Rückkopplung, Einfluss auf Verstärkung, Zeitkonstanten, Invertierender und Nichtinvertierender Verstärker
- 2 Grundlegende Verstärker-Schaltungen und grundlegende Bauteile: CMOS Verstärker (Common Source), Cascode, Source-Folger
- 3 Halbleiter, Diode, MOSFET (DC, AC, Rauschen, Matching)
- 3ü Bipolar Transistor, MOS-Kondensator, Schwache Inversion, BSIM-Modell
- 4 AC Analyse (Frequenzverhalten der Schaltungen), Übertragungsfunktion für Schaltungen mit Kondensatoren, Bestimmung von dominanten Zeitkonstanten (RC Regel), Methode der Nullimpedanzen
- 4ü Common Source Verstärker
- 4ü Single Ended Verstärker, Kaskaden und Kaskoden
- 5 Einfluss von Rückkopplung auf Zeitkonstanten, Stabilität, Nyquist Regel
- 5ü Transimpedanz Verstärker, Spannungsregler
- 7 Komplexere Verstärker, Einstufig, Zweistufig, Rail to Rail, Volldifferentiell, Klasse AB
- 8 Komparatoren
- 9 Switched Capacitor Schaltungen
- 10 Filter (RC, Gm-C, Switched Capacitive Filter)
- 11 ADCs (Dual und Single Slope, Flash, Subranging, SAR mit Kondensatoren, SAR mit Stromquellen, SAR Asynchron, Sigma Delta, Zyklisch mit Stromzellen, Zyklisch mit Switched Capacitive Schaltungen)
- 12 Spannungsreferenz, PLL und VCO, LVDS Treiber, LVDS Empfänger

- Was haben wir gelernt?
- Es geht um analoges Chipdesign
- Chipdesignsoftware Cadence – Übungen
- Analoges Designflow: Schaltungsentwurf, Simulation (AC, DC, Transiente Simulation, Rauschen, Matching), Layoutentwurf, DRC, LVS
- Digitales Designflow: HDL Code, Simulation -> (automatische) RTL Synthese, Simulation (Standard-Logikzellen) -> Layout-Synthese, Simulation
- Am Anfang des Projekts muss man Hersteller (foundry, vendor) und Technologie wählen, PDK (Process Design Kit) (Technologiespezifische Bibliotheken fürs Cadence) besorgen
- Europractice
- Transistorherstellung siehe Link
- Chipprojekte sind hierarchisch aufgebaut
- Grundbausteine: Common Source, Cascode, Source Follower, Current Mirror, Differenzpaar
- Widerstände selten benutzt – Alternative ist C
- Transistormodelle sind sehr komplex – BSIM Model
- Fragen
- Welche Chiphersteller kennen wir?
- AMS, TSMC, UMC, IBM, GF, LF, XFAB...
- Welche Prozesse?
- CMOS, SOI, HVCMOS, FINFET, BCD, BiCMOS
- Welche „process nodes“: 0.35, 0.24, 0.18, 0.13, 90nm, 65nm, 45nm...
- Das meistbenutzte MOSFET-Modell: BSIM
- Welche Firmen sind fürs Leiterplattendesign nützlich? PCB pool, Farnel

- Vielen Dank für Ihre Aufmerksamkeit

